## INITIAL SETTING-UP

This section is intended for the engineer who is installing the equipment and presumes the same background as the INSTALLATION section.

Some of the preset controls and switches are also mentioned in the operating instructions, but it is usually not recommended that the operator carry out any setting-up unless specificly instructed what to do.

NOTE! Many of the switches and jumpers affect the operation of the system and must be set accordingly.

A guide on how to select the boards and assemblies to make up a system is given in section CONFIGURATION. That section will also show how the switches and jumpers must be set according to the system. A sample of an order form is included.

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## INITIAL SETTING UP

### EXTERNAL PRESETS

Six controls on the back panel of the display unit must be set in the positions that bring the display in accordance with the system in which it is to operate.

They are as follows:

-SPEED SELECT determines the baud rate used in the Asynchronous Interface. A table on the back panel gives switch positions and baud rates.

-NO PARITY switch must be set to NO if checking of received data and adding of parity bit to transmitted data is required.

-EVEN PARITY chooses between even or odd parity. The switch is effective only when the NO PARITY switch is in the NO position.

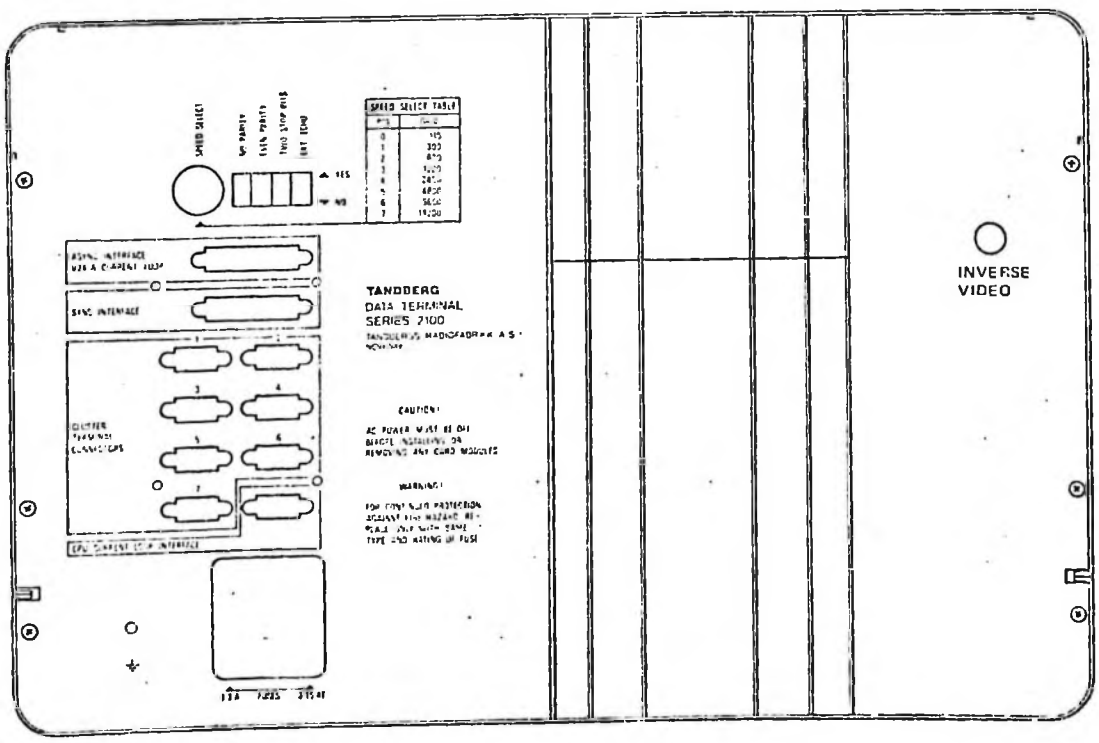
NOTE!
Always switch the power off when setting the switches.

-TWO STOP BITS switch must be set to agree with the number of stop bits used in the system.

-EXT.ECHO switch must be set in the NO position when the link is half duplex.

-INVERSE VIDEO can be obtained by depressing a switch on the Display Logic 2 board. A hole in the right hand back panel gives access to the switch.

The figure below shows the position of the six controls on the back panels.



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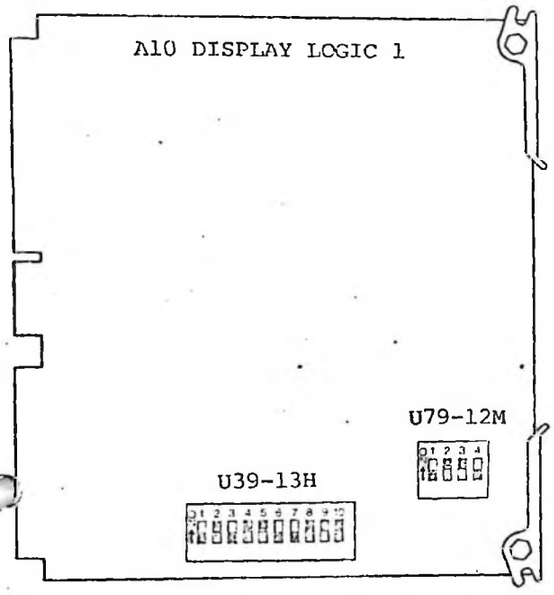
## INTERNAL PRESETS

The internal presets, also called factory presets, are either switches or jumpers. To reach them the different boards must be removed from the racks.

NOTE!
Always switch the power off when removing or inserting the boards!

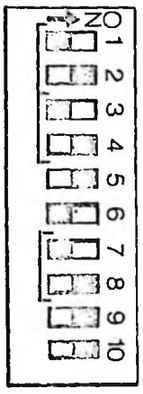
### DISPLAY LOGIC 1

Unless otherwise specified when ordering, the switches on the Display Logic I board will be set as shown in the figure below:




The separate switches of U39 and U79 can only switch on and off, therefore two separate ones must be employed to form a toggle switch. The two switches forming a toggle switch must alway be in opposite positions.
(Marked with ⌊___⌋ on the fig.)

The setting of U39 is shown in the standard TDV 2114 version:




SYN CODE
CLEAR KEY
ON LINE BY CARRIER
ON LINE BY DSR.
ON:CPU MODE, OFF:TELETYPE MODE
ON LINE
ON LINE BY RECEIVE EN.
ON LINE BY BOTH REC./TRANSM.EN.
ROLL MODE
ON:7 BIT WORD LENGTH
OFF:8 BIT WORD LENGTH

The numbers in the following text refer to switch numbers.

1 and 2: Selectable Clear Selects whether the ACK, NAK and ENQUIRY indicators shall be switched off with the CLEAR key or the SYN code.

3 and 4: Select whether to go ON LINE by carrier wave or data set ready.

5: Selects either the CPU mode or the Teletype mode (must be in CPU mode whenever a CPU board is present.

6: If ON, the unit will always be ON LINE and the TRANS and LINE keys inhibited.

7 and 8: Select whether to go ON LINE by Reiceve Enable alone or by both Receive and Transmit Enable.

9: Prevents automatic ROLL UP in the OFF position. The roll up/down codes are not inhibited.

10: Selects either 7 or 8 bit word length.

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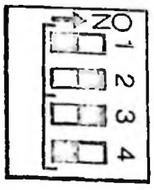
The setting of U79 shown in the standard TDV 2114 version:




RQTS.ONLY BY TRANS KEY.
RQTS.ALSO BY LINE KEY.
NORMAL CURRENT LOOP
SYSTEM CURRENT LOOP

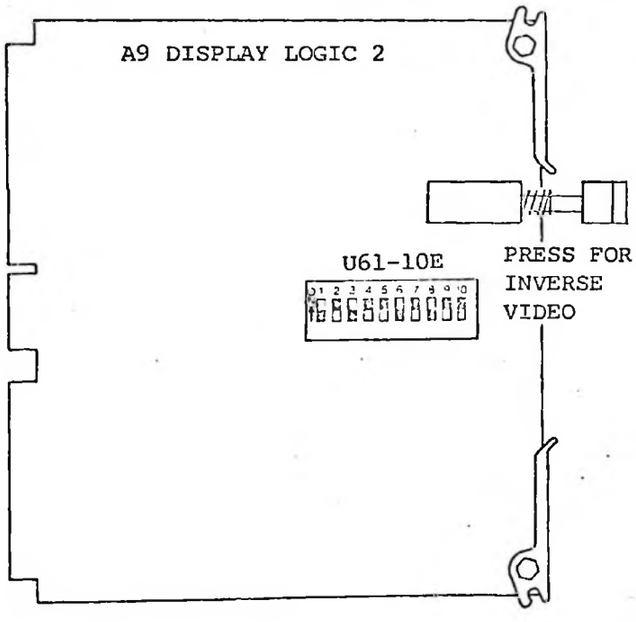
The numbers in the following text refer to switch numbers.

1 and 2: Select whether to request to go on line by TRANS key alone or by TRANS key and LINE key.

3 and 4: Select between a 47ohm resistor or a 10V zener diode in series with the current loop.

DISPLAY LOGIC 2

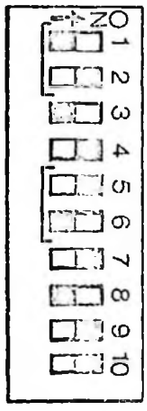
Unless otherwise specified when ordering, the switches on the Display Logic 2 board will be set as shown in the figure below:




The INVERSE VIDEO push switch is located to the right of switch U61.

Switches marked ⌊⌋ must always be in opposite positions because of their toggle function.

The setting of U61 shown in the standard TDV 2114 version:




DOT 9=0 (BLANK)
DOT 9=DOT 8
AUTOMATIC CR./LF.INHIBIT
ON:ATTRIBUTE MODE, OFF:UNDERLINE MODE
CURSOR BLINK
STEADY CURSOR
ATTRIBUTE BYTE CLEAR
NOT CONNECTED
CONTROL CODE CLEAR
ON:UNDERSCORE CURSOR
OFF:BLOCK CURSOR

The numbers in the following text refer to switch numbers.

1 and 2: Select whether dot 9 in a character space shall be zero (blank) or like dot 8. (Only with semigraphic PROM).

3: Inhibits automatic carriage return and line feed in the ON position.

4: Selects between Attribute mode or Underline mode.

5 and 6: Select between blinking or steady cursor.

7: The attribute character will not be displayed in the ON position.

8: Not connected.

9: When ON, inhibits the displaying of the control code neccessary when two character generators are used.

10: Selects between Underscore cursor and Block cursor.

NOTE!
Switches 4 and 7 must always be in the ON or OFF position simultaneously.

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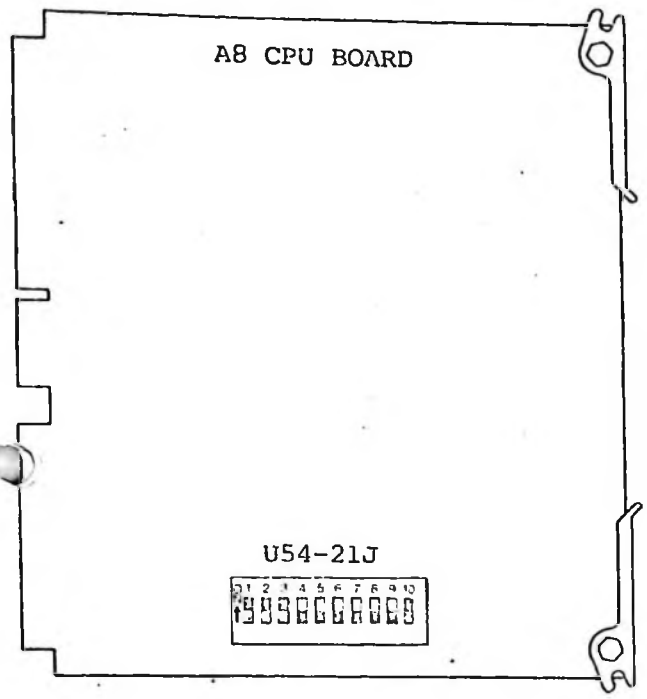
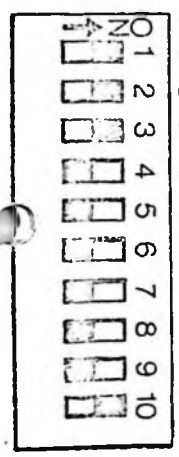
CPU BOARD

Unless otherwise specified when ordering, the switches on the CPU board will be set as shown in the figure below:




The setting of U54 shown in the standard TDV 2114 version:




ON:7 BIT WORD LENGTH
OFF:S BIT WORD LENGTH
ON:PARITY CHECK, OFF:NO PARITY CHECK
9600 BAUD
4800 BAUD
2400 BAUD
1200 BAUD
600 BAUD
300 BAUD
75/110 BAUD DISABLE
110 BAUD DISABLE

The numbers in the following text refer to switch numbers.

1: Selects either 7 or 8 bit word length.

2: Selects whether to check parity or not.

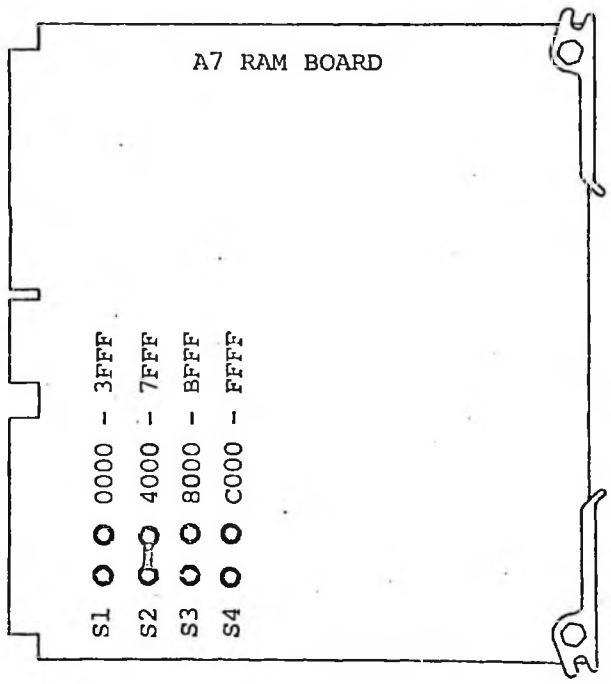
3 to 8: Set desired data transfer rate of the Printer and Test Interface.

9: Sets the data transfer rate to 110 baud when switch 10 is OFF, to 75 baud when switch 10 is ON.

10: Inhibits the 110 baud rate of switch 9 when ON.

RAM BOARD

Unless otherwise specified when ordering, the switches on the RAM board will be set as follows:
The first 16k module from C000-FFFF.
The ~~next~~ Last 16k module from 4000-7FFF.
The ~~last~~ NEXT 16k module from 8000-BFFF.




The Memory Allocation Switch can be set in one of four possible positions.

| Position | Memory Allocation |
|---|---|
| S1 | 0000-3FFF |
| S2 | 4000-7FFF |
| S3 | 8000-BFFF |
| S4 | C000-FFFF |

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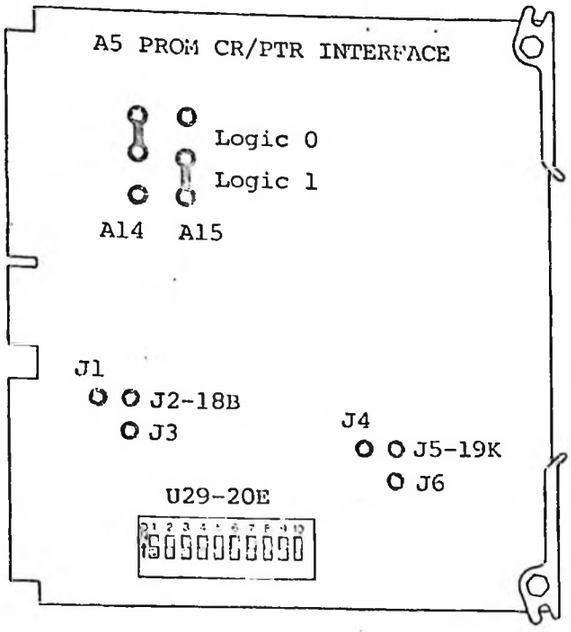
PROM CR/PTR INTERFACE




The Memory Allocation Switch consists of two jumpers that can be positioned four different ways to obtain the desired memory allocation.
See table below:

| Memory Allocation | A14 | A15 |
|---|---|---|
| 0000-3FFF | 0 | 0 |
| 4000-7FFF | 1 | 0 |
| 8000-BFFF | 0 | 1 |
| C000-FFFF | 1 | 1 |

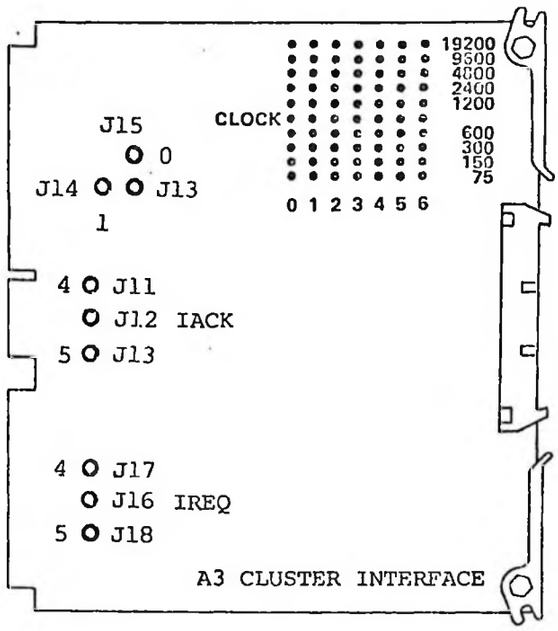
If one or two 8-bit Card Readers (CR) are to be used, the ST1 jumper must be in position J2-J3. Jumper CP1 must be in position J4-J5. All the switches in the DIP switch must be ON.

If one 12-bit CR is used, pins 20 and 21 and P2 must be connected together.

If a Paper Tape Reader (PTR) is to be used, the ST1 jumper must be in position J1-J2. Jumper CP1 must be in position J5-J6.

If a Synchronous Interface board is in use, only one 8-bit CR can be used, and all the switches in U29 must be OFF.

CLUSTER INTERFACE




The setting of the jumpers on the Cluster Interface depends on whether the system consists of one or two Cluster Interface boards.

The device code for a one board system goes from 00 to 0F (hex) and the IREQ/IACK jumpers must be set in the "4" position. The jumper in position 5D on the board must be set between J13 and J15 (0) which is the position corresponding with IREQ/IACK 4. This board must be placed in position A3 in the board rack.

If a second Cluster Interface board is used, the IREQ/IACK jumpers must be set in the "5" position. The jumper in position 5D on the board must be set between J13 and J14 (1) which is the position corresponding with IREQ/IACK 5. The device code for this Cluster Interface goes from 80 to 8F (hex) and it must be placed in the A6 position in the board rack. The cable to the external devices is plugged directly into J3 on the board, it does not go via the Connector board as for the Cluster Interface in position A3.

Continued next page.

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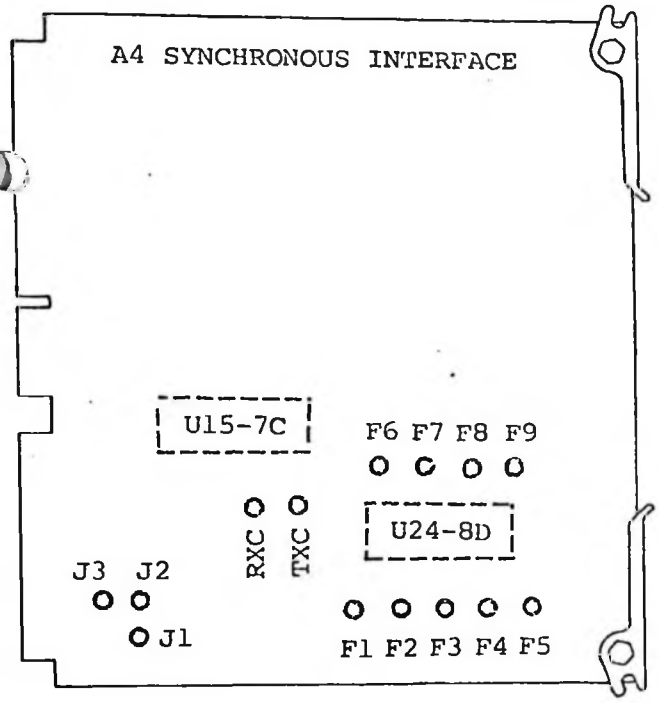
The transfer rate of the seven input/ output UARTs can be individually determined. The center pin of each wafer is the clock output for each UART and must be wire-wrapped to the pin on the same wafer that represents the desired baud rate.

SYNCHRONOUS INTERFACE




The signal Output Interrupt Enable (OIE) is connected to a pull-up resistor through the printed circuit. Provisions are however made so that OIE may be generated by a flip-flop. Such a version of the Synchronous Interface will be equipped with a jumper in position J1 to J2.

NOTE!
The printed wire between J2 and J3 must be cut if the jumper is in position J1 to J2.

In the synchronous mode, the USART gets its transmitting and receiving clock frequencies from the modem on the CT114 and CT115 lines. In the asynchronous mode, the clock frequencies are supplied by the counter U24. The desired clockfrequencies can be connected to RXC and TXC by soldering in a wire. The table below shows the counter outputs with corresponding frequencies in kilohertz.

| F1 | F2 | F3 | F4 | F5 | F6 | F7 | F8 | F9 |
|---|---|---|---|---|---|---|---|---|
| 307,2 | 153,6 | 76,8 | 38,4 | 19,2 | 9,6 | 4,8 | 2,4 | 1,2 |

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