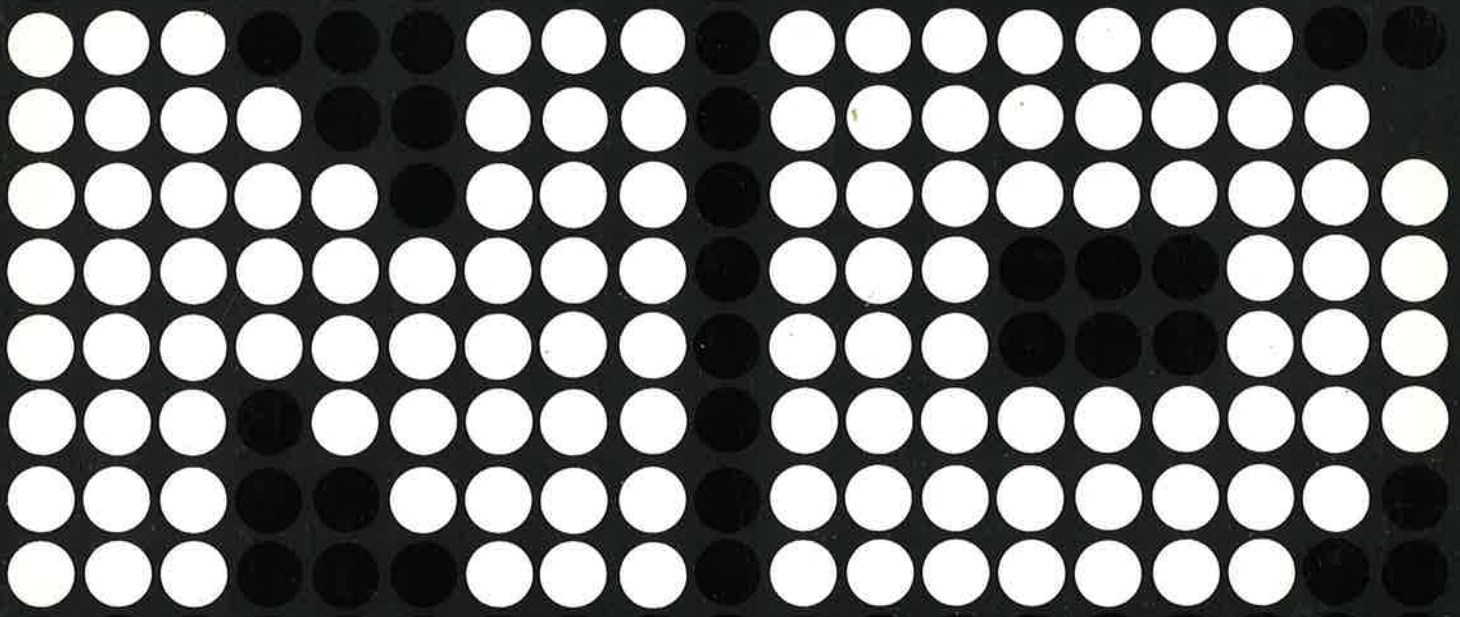
CIRCUIT DIAGRAM SYMBOLS

A/S NORSK DATA-ELEKTRONIKK



CIRCUIT DIAGRAM

SYMBOLS

July, 1976

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1 INTRODUCTION

The paragraphs below describe the rules used in obtaining logic expressions and definitions of logic signals and the symbols used to represent logic elements in our circuit diagrams. The system is based on elements of the NAND/NOR family, which is now most common in use. It is also supposed to be NPN elements with positive supply voltage.

2 LOGIC EXPRESSIONS

The two states of the binary variable as represented by a voltage in the circuit system are defined as follows:

State 0 : V < 0,4 volt or "low"
State 1 : V > 2,4 volt or "high"
Undefined : 0,4 volt < V < 2,4 volt

The state of a variable under given conditions is indicated by index 0 or 1 respectively. Index 1 may be omitted, so that A and A_1 are identical.

Example 1

ADD_0 : The signal is low when the instruction ADD is present (decoded from the instruction register).

Example 2

$ADD = IR15_0\ 14_1\ 13_1\ 12_0\ 11_0$

The signal ADD is decoded from the instruction register, IR, bits 11 through 15 and is "true" when IR15=IR12=IR11=0 and IR14= IR13=1.

The symbols used for the logic operations "AND" and "OR" are the standard arithmetic multiplication and addition symbols, including the rule for omitting the multiplication sign.

Example 3

$A \cdot B_0 \cdot C$ or $A_1 \cdot B_0 \cdot C_1$ or $A_1 B_0 C_1$

$D+E+F_0$ or $D_1+E_1+F_0$

$(A_0 B_1 + A_1 B_0)\ (C_0 D_1 + C_1 D_0)$

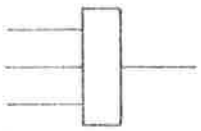
The "name" of triggering signals should be chosen to reflect the active state of that signal, which means that a signal which is active when it is high should have index 1 and a signal which is quiescent when it is high should have index 0.

Example 4

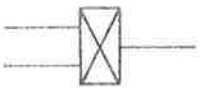
The clock input to a SN7474 flip-flop is requiring a positive pulse and may be called AS1. The clear input to the same flip-flop requires a negative going pulse and should be labelled $AS2_0$.

3 LOGIC ELEMENTS

The symbols used for logic elements are a result from several years of experience in design and manufacture of digital systems. The symbol for a "NAND" gate is shown as such, and no attempt is made to reduce the diagram to a system containing the basic family of AND/OR/INVERT elements. A "NAND" element is a "NAND" element, and one single element is frequently used for both "AND" and "OR" functions simultanously.



3-input NAND

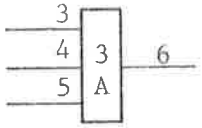


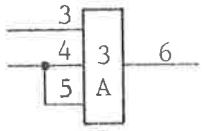
2-input NOR

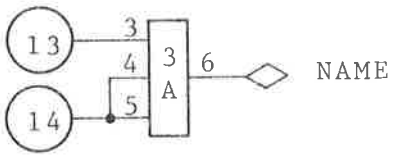
The selected symbols shown above are used for the basic logic elements, NAND and NOR, which together make a complete logic family. The symbols are chosen for compactness and ease of drawing, and consist of straight lines only. The logic diagrams of course become completely circuit oriented, and corresponds one to one with the actual hardware.

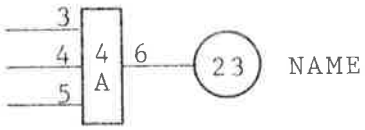
4 CIRCUIT DIAGRAMS

All circuit elements are mounted on printed circuit boards. The position of the circuit on this board is shown by the coordinates of the circuit, column first, identified by a number and then row, identified by one of the letters A, B, C, D.. . These coordinates together with the pin number of the circuit package are shown in the logic diagrams.









Input terminals are if possible to the left and output to the right. The distance between input lines should be 5 mm. If an unused input terminal is connected to a used terminal this should be shown in the diagram. Circled numbers represent card terminals.

Instead of connecting an output signal to another circuit or an output terminal the signal line may be terminated in a diamond head and given a name. This name usually occurs as input signal other places in the diagram.

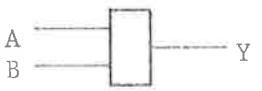
Example

Pin 11 of the circuit in position 2B is referred to as 2B11.

5 SYMBOLS FOR TI SERIES 74N CIRCUITS

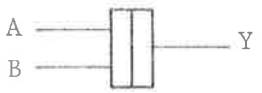
The main integrated circuit family used by ND is the Texas Instrument Series 74N, and a complete list of the standard symbol (TI's) and ND's corresponding symbol is given below.

7400
Quadruple 2-input NAND gate



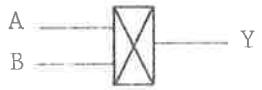
$Y=\overline{A \cdot B}$

7401
Quadruple 2-input NAND gate with open collector output



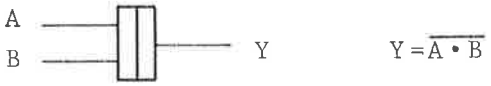
$Y=\overline{A \cdot B}$

7402
Quadruple 2-input NOR gate

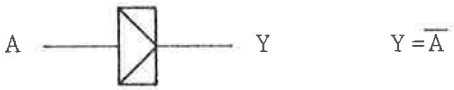


$Y=\overline{A+B}$

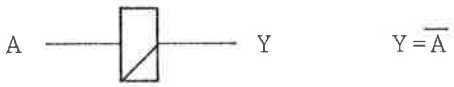
7403
Quadruple 2-input NAND gate
with open collector output



7404
Hex inverter

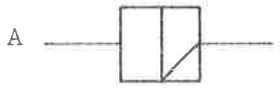


7405
Hex inverter with open collector output



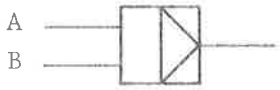
7406
Hex inverter buffer/driver with open-
collector high-voltage output

7407
Hex buffer/driver with open-collector high-voltage output



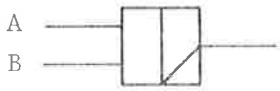
$Y = A$

7408
Quadruple 2-input AND gate



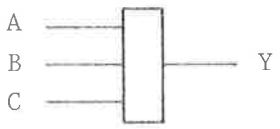
$Y = A \cdot B$

7409
Quadruple 2-input positive AND gate with open-collector output



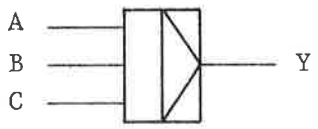
$Y = A \cdot B$

7410
Triple 3-input NAND gate



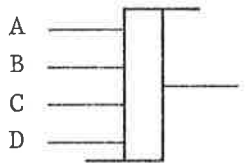
$Y = \overline{A \cdot B \cdot C}$

74H11
Triple 3-input AND gate



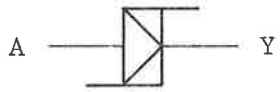
$Y = A \cdot B \cdot C$

7413
Dual 4-input NAND Schmitt trigger



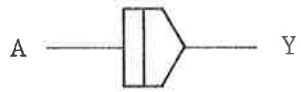
$Y = \overline{A \cdot B \cdot C \cdot D}$

7414
Hex Schmitt-trigger inverter



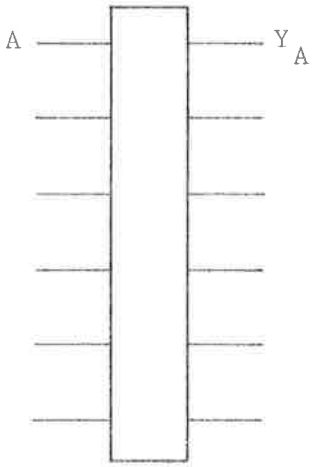
$Y = \overline{A}$

7416
Hex inverter buffer/driver with open-collector high-voltage output



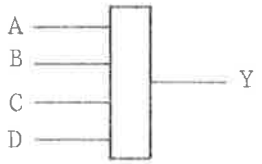
$Y = \overline{A}$

7417
Hex buffer/driver with open-collector high-voltage output



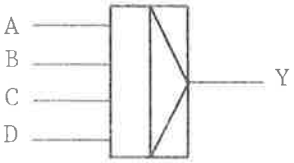
$Y_A = A$

7420
Dual 4-input NAND gate



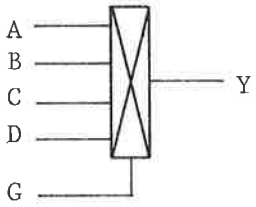
$Y = \overline{A \cdot B \cdot C \cdot D}$

74H21
Dual 4-input AND gate



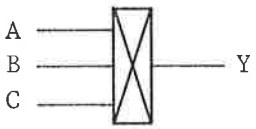
$Y = A \cdot B \cdot C \cdot D$

7425
Dual 4-input NOR gate with strobe



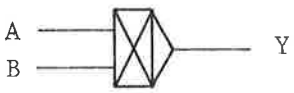
$Y=\overline{G(A+B+C+D)}$

7427
Triple 3-input NOR gate



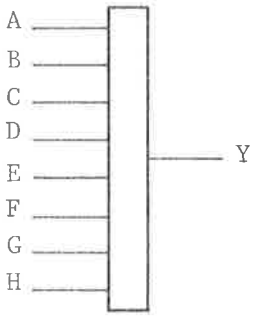
$Y=\overline{A+B+C}$

7428
Quadruple 2-input NOR buffer



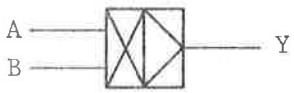
$Y=\overline{A+B}$

7430
8-input NAND gate



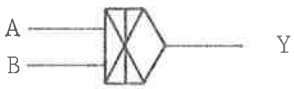
$Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H}$

7432
Quadruple 2-input OR gate



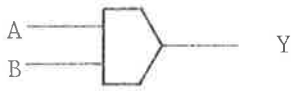
$Y = A + B$

7433
Quadruple 2-input NOR buffer
with open-collector



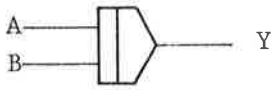
$Y = \overline{A + B}$

7437
Quadruple 2-input NAND buffer



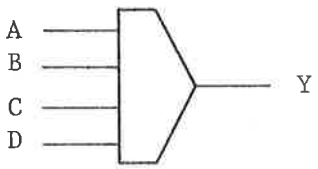
$Y = \overline{A \cdot B}$

7438
Quadruple 2-input NAND buffer with open-collector



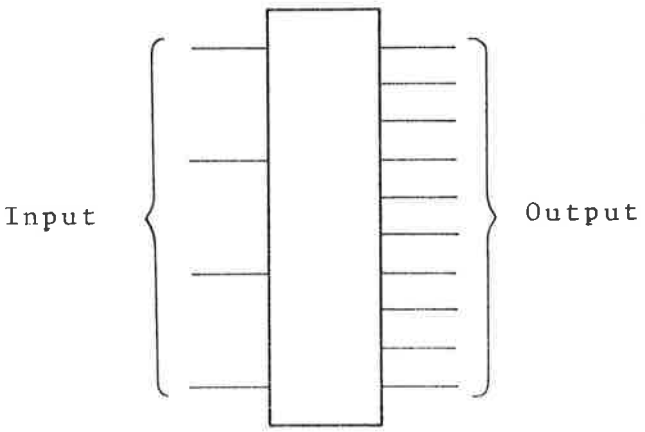
$Y=\overline{A \cdot B}$

7440
Dual 4-input NAND buffer

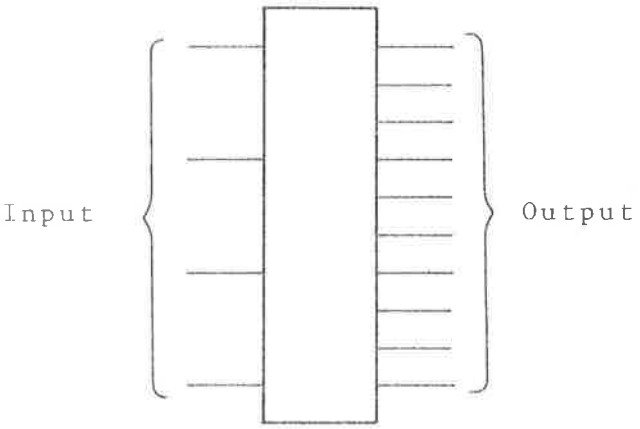


$Y=\overline{A \cdot B \cdot C \cdot D}$

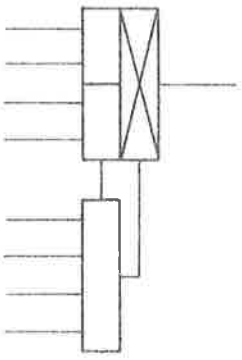
7442
4-line-to-10-line decoders (1-of-10)



7445
BCD to decimal decoder/driver with
open-collector outputs

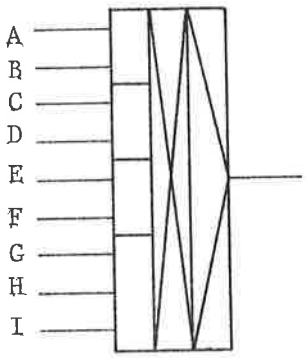


7450 - 7451 - 7460
2x2 AND-OR-INVERT



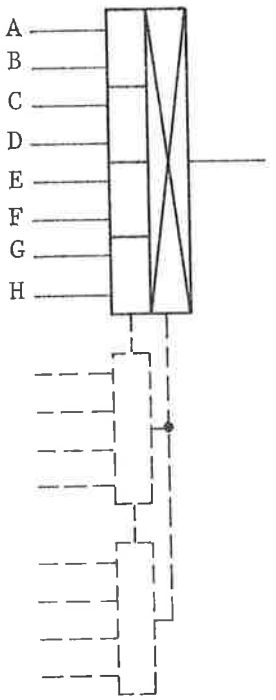
The four-input gates are 7460 circuits

74H52
Expandable 4-wide AND-OR gates



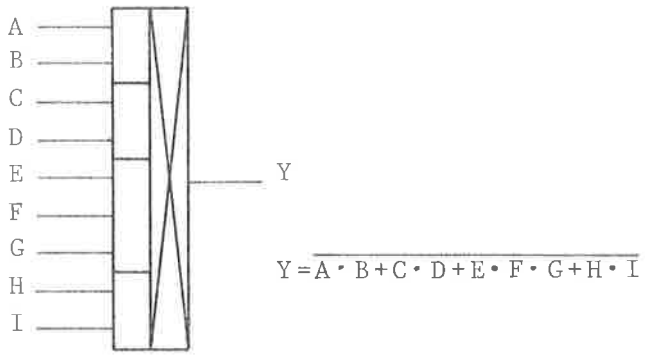
$Y = A \cdot B + C \cdot D + E \cdot F + G \cdot H \cdot I$

7453 - 7454
4x2 AND-OR-INVERT

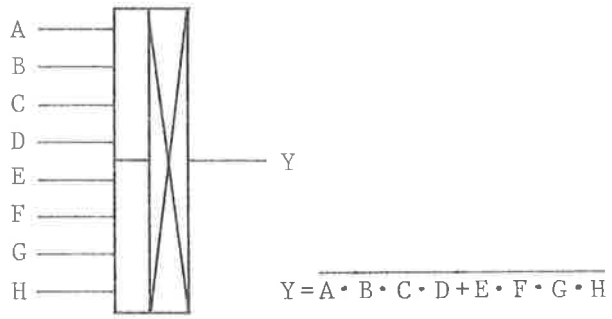


$Y = \overline{A \cdot B + C \cdot D + E \cdot F + G \cdot H}$

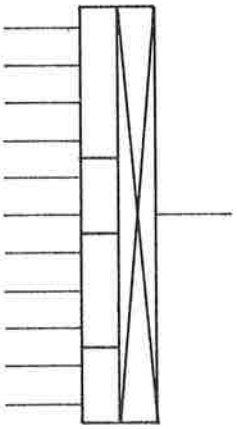
74H54
Expandable 2-2-2-3 - input
AND-OR-INVERT gates



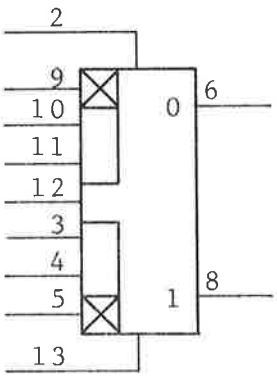
74H55
2-wide 4-input AND-OR-INVERT gates



74S64
4-2-3-2 - input AND-OR-invert gates

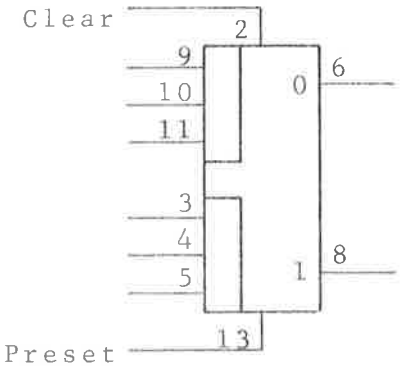


7470
J-K flip-flop

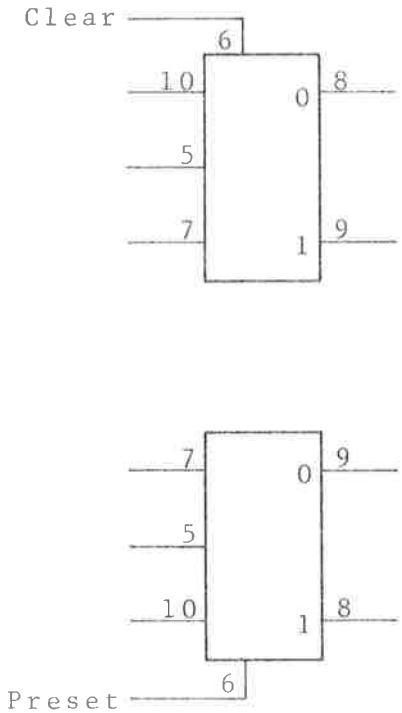


The AND gate opposite the 0 output is equal to K-inputs. The preset and clear input is pointing to that side of the flip-flop which becomes "high" for a corresponding "low" pulse.

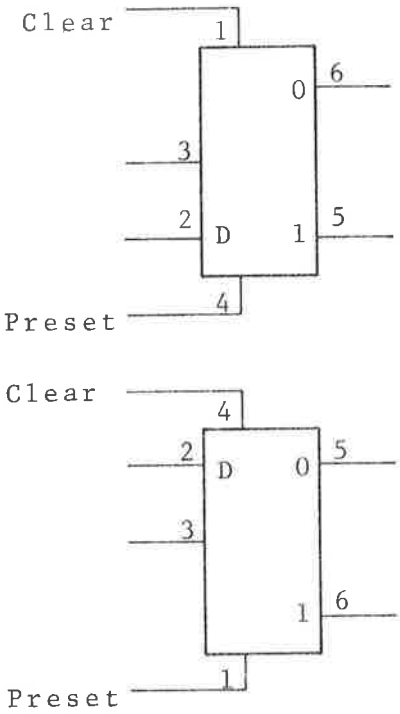
7472
J-K master-slave flip-flop



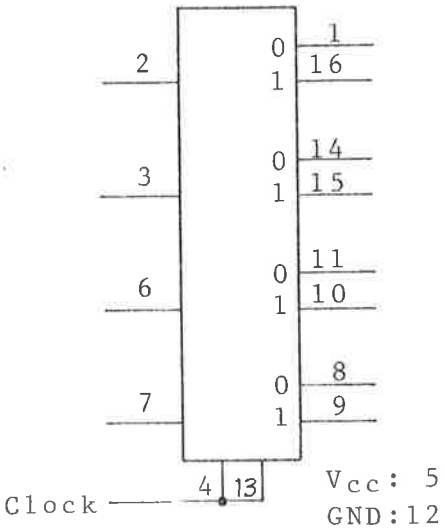
7473
Dual J-K master-slave flip-flop



7474
Dual D-type edge-triggered flip-flop

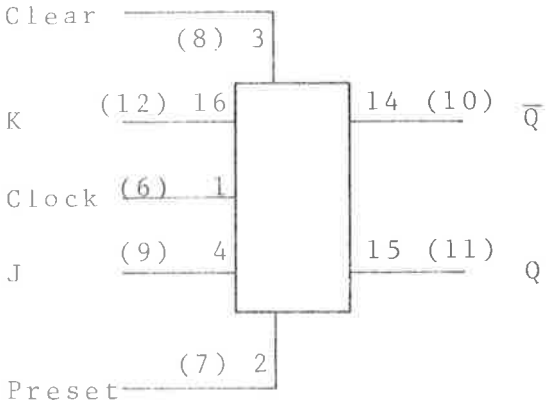


7475
Quadruple bistable latch

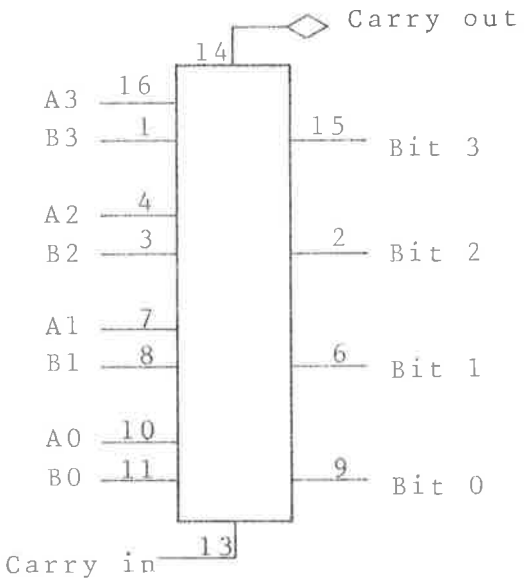


The clock input on pins 4 and 13

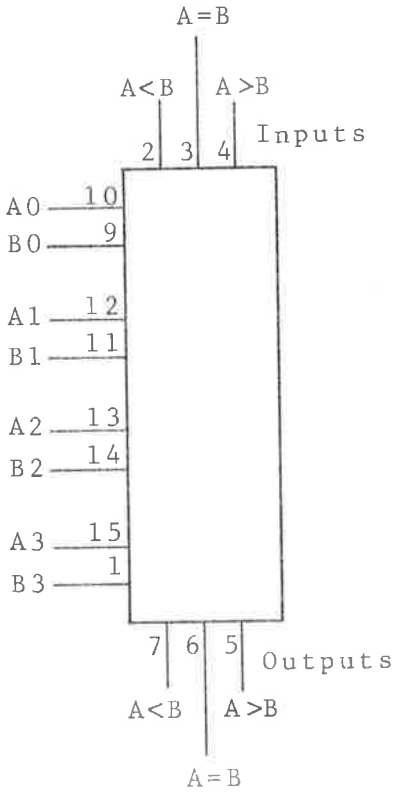
7476
Dual J-K flip-flop with Preset and Clear



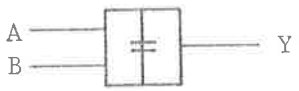
7483
4-bits binary full-adder



7485
4-bit comparator



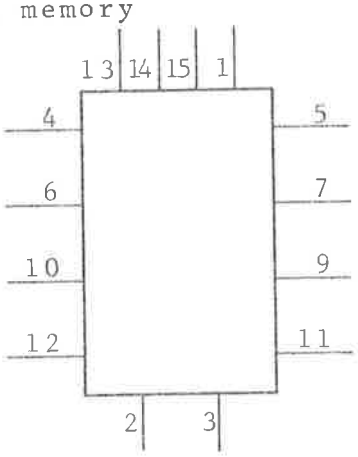
7486
Quadruple 2-input exclusive-OR-element



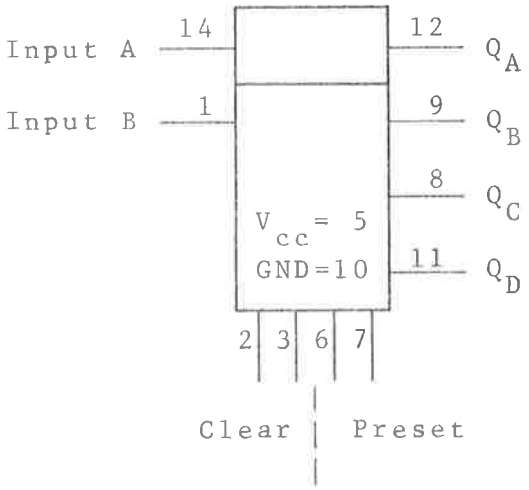
$Y = A \oplus B$

$= \overline{A} \cdot B + A \cdot \overline{B}$

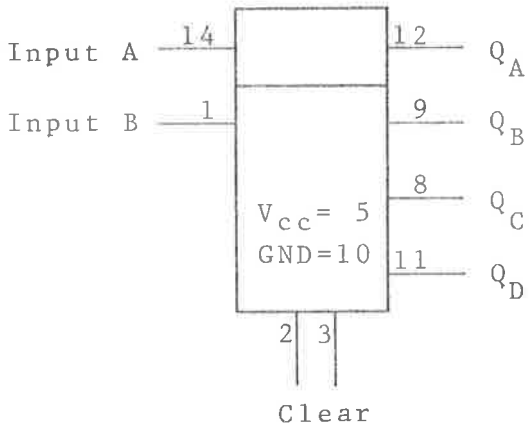
7489
64-bit read/write memory



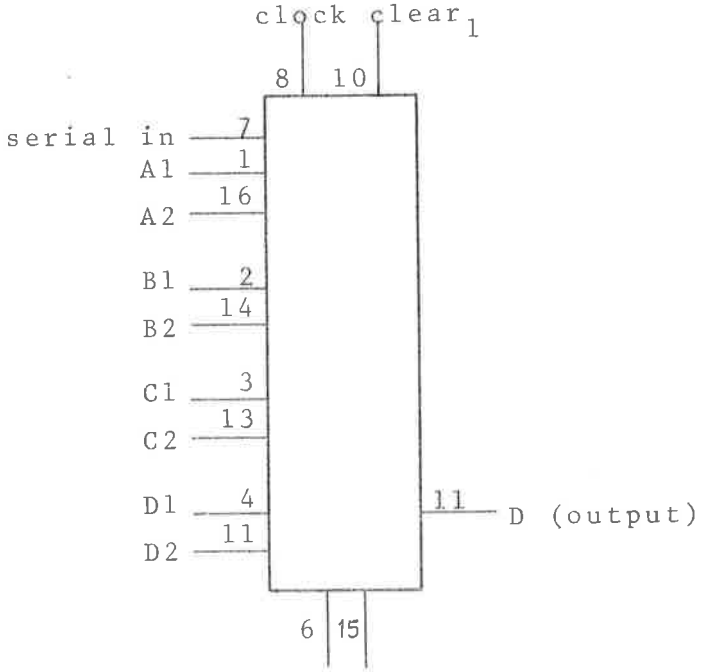
7490
Decode counter



7493
4-bit binary counter

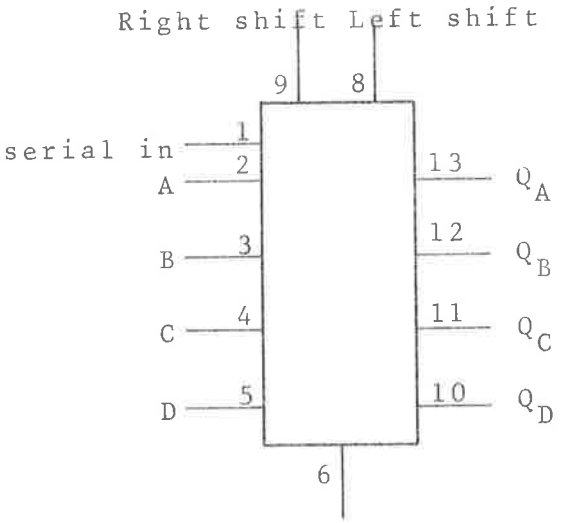


7494
4-bit shift register



+5V = 5
GND = 12

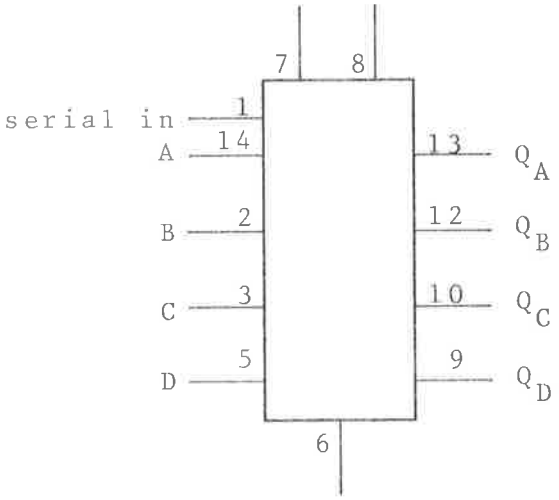
7495
4-bit right-shift, left-shift register



Mode Control:

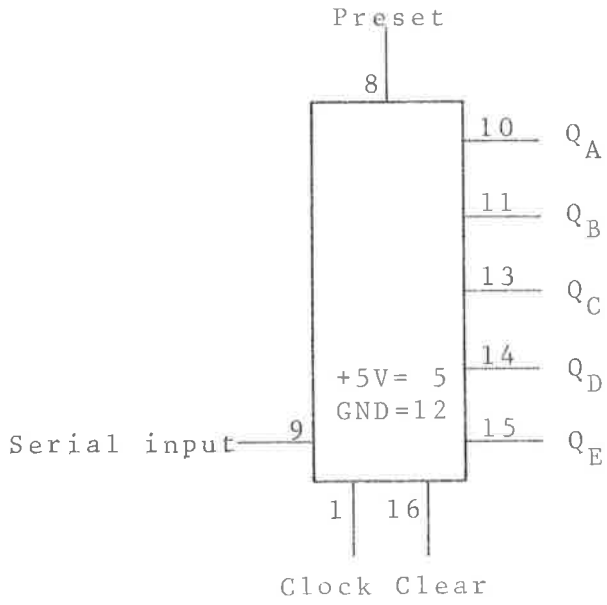
0 = Shift serial
1 = Shift parallel

74L95
4-bit parallel-access shift register

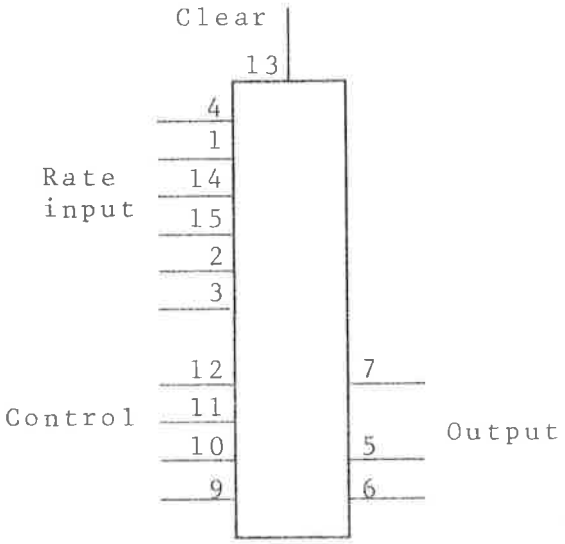


+5V = 4
GND = 11

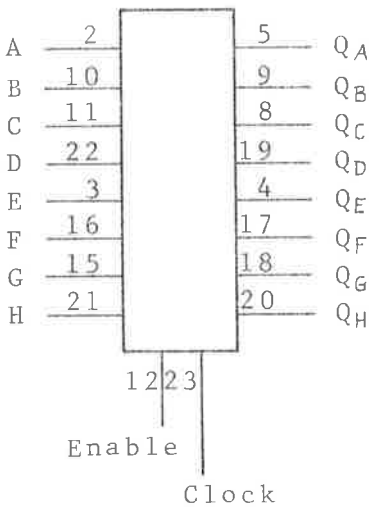
7496
5-bit shift register



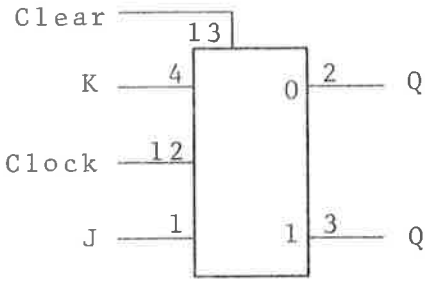
7497
Synchronous 6-bit binary rate multiplier



74100
8-bit bistable latches

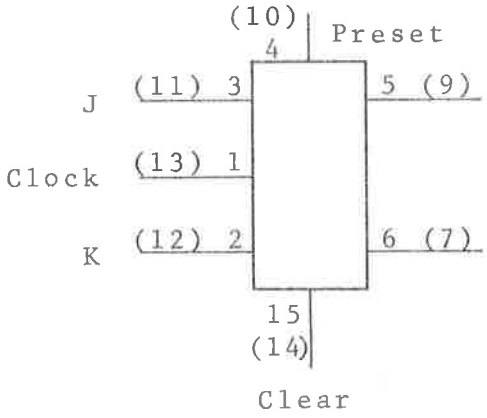


74107
Dual J-K Master-Slave flip-flop

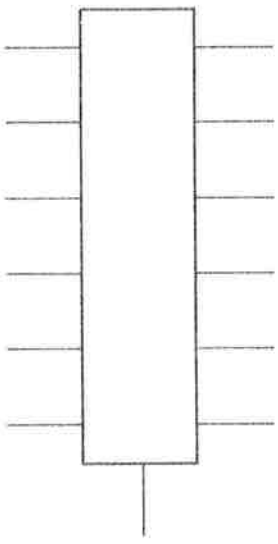


J	K	Q	$\overline{Q}$
L	L	No	toggle
H	L	H	L
L	H	L	H
H	H	Toggle	

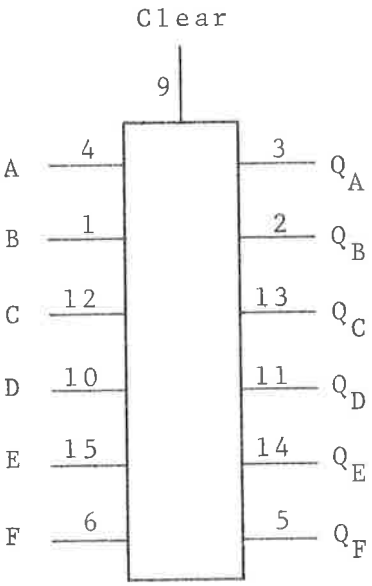
74S112
Dual J-K negative-edge-triggered
flip-flop with preset and clear



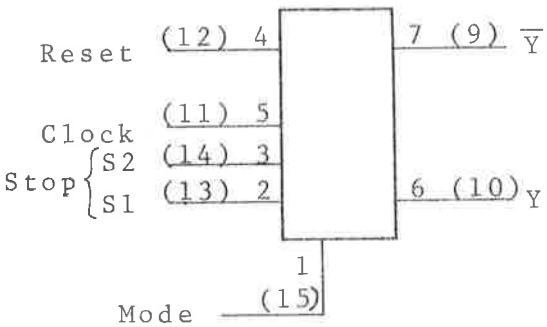
74S114
Dual J-K negative-edge-triggered
flip-flop with preset, common clear
and common clock



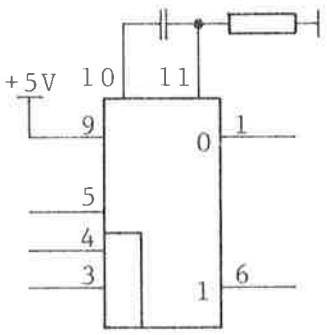
74118
6-bit set latch



74120
Pulse synchronizer

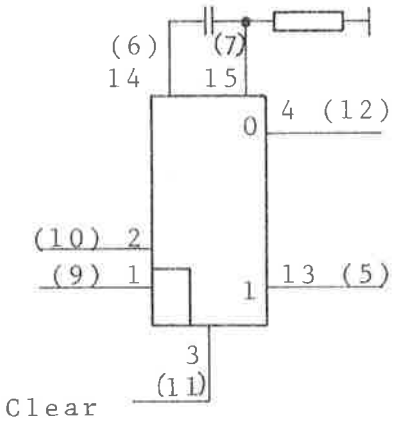


74121
Monostable multivibrator



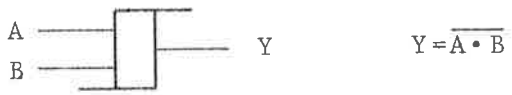
$T \approx 0,7 \cdot RC$
Rmin = 1.4 kΩ
Rmax = 40 kΩ

74123
Retriggerable monostable multivibrator with clear

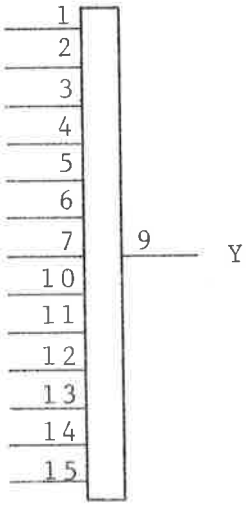


$T \approx 0.32 \cdot RC$
Rmin = 5 kΩ
Rmax = 50 kΩ

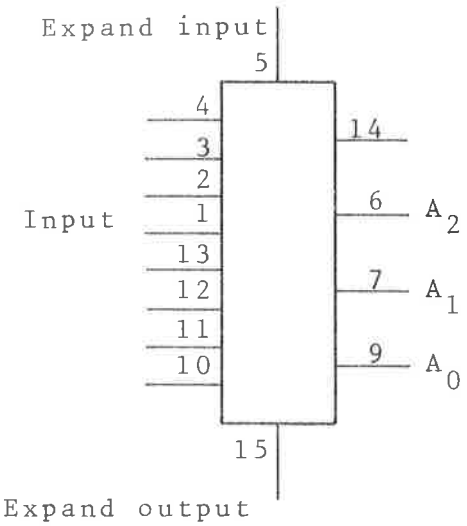
74132
Quadruple 2-input positive NAND
Schmitt trigger



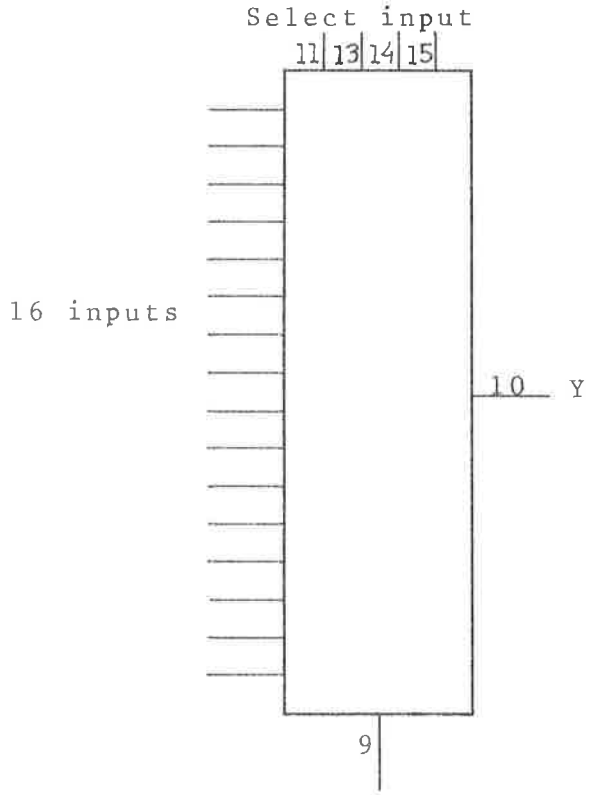
74S133
13-input positive NAND gate



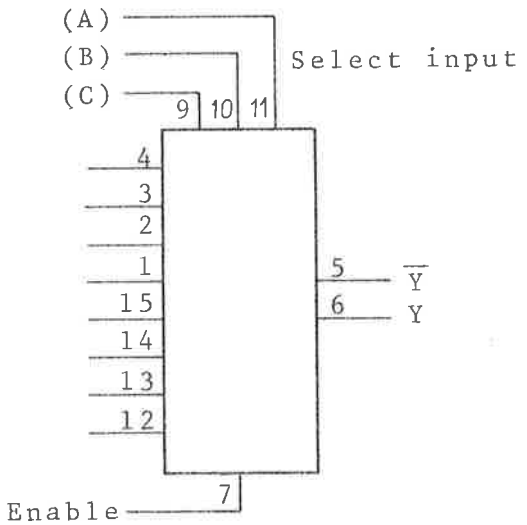
74148 (Equal to 9318)
8-line-to-3-line priority encoder



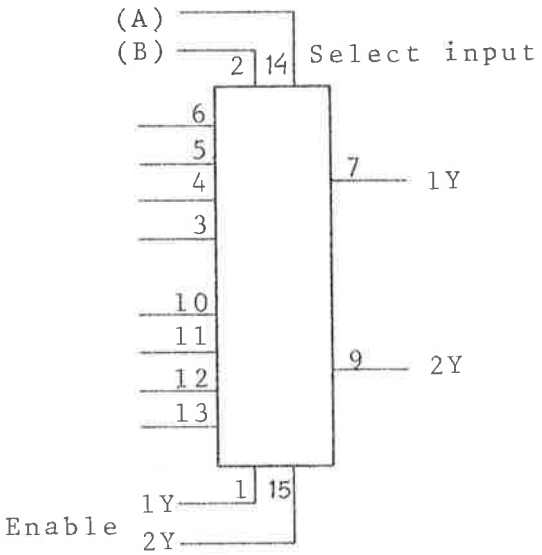
74150
Data selector/multiplexer 16-1



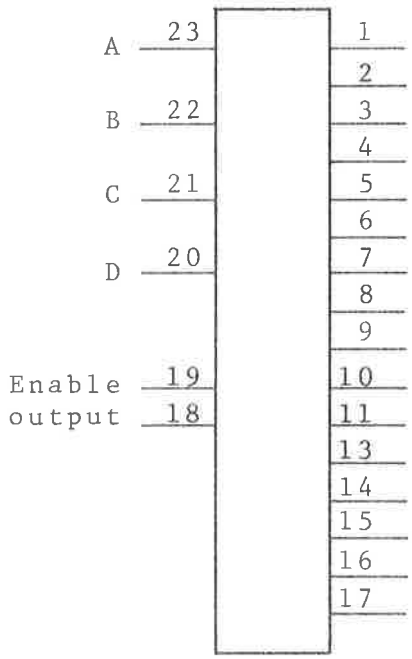
74151
Data selector/multiplexer 8-1



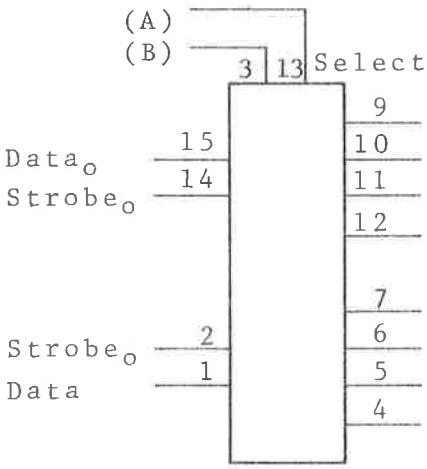
74153
Dual 4-line-to-1-line data selector/
multiplexer



74154
4-line-to-16-line decoder/demultiplexer

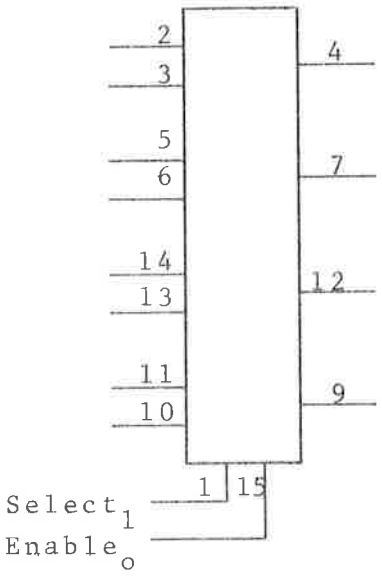


74155
Dual 2-line-to-4-line decoder/demultiplexer



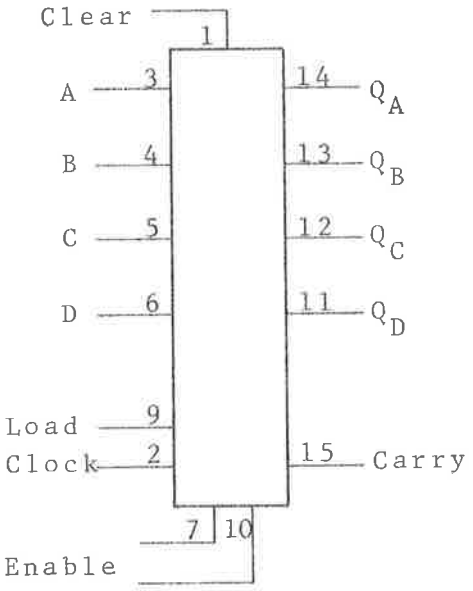
74156 is equal to 74155

74157/74158
Quadruple 2-line-to-1 line data selector/multiplexer

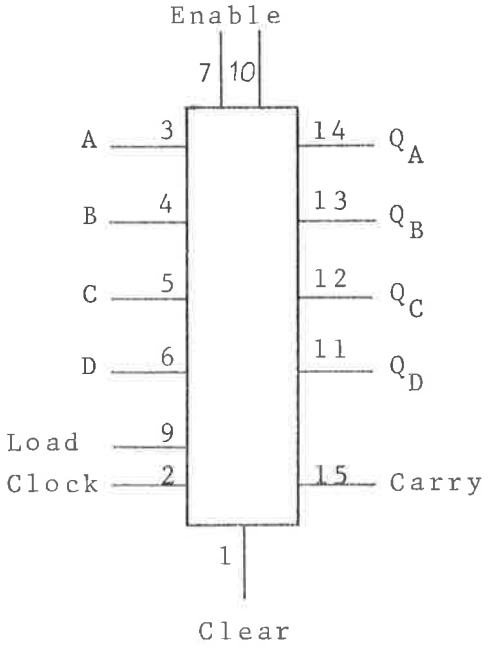


74158 has inverted output

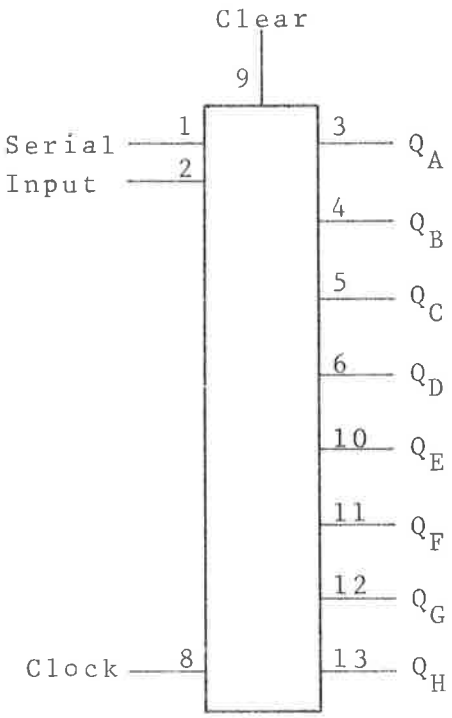
74161
Synchronous 4-bit counter



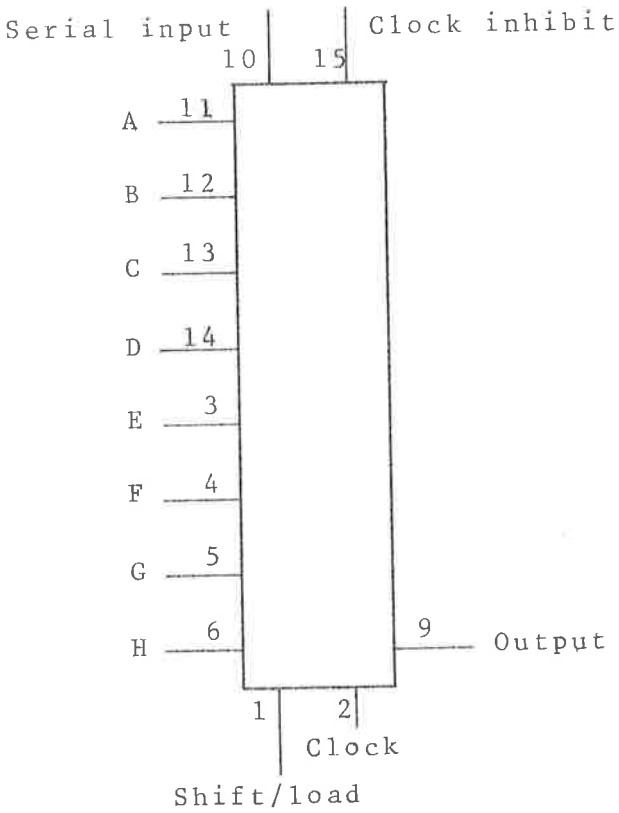
74163
Fully synchronous binary counter



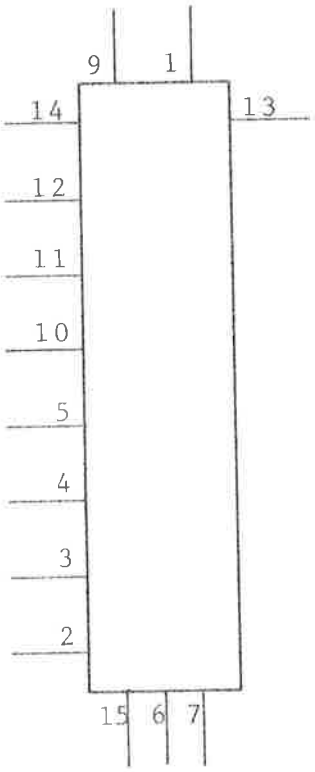
74164
8-bit shift register



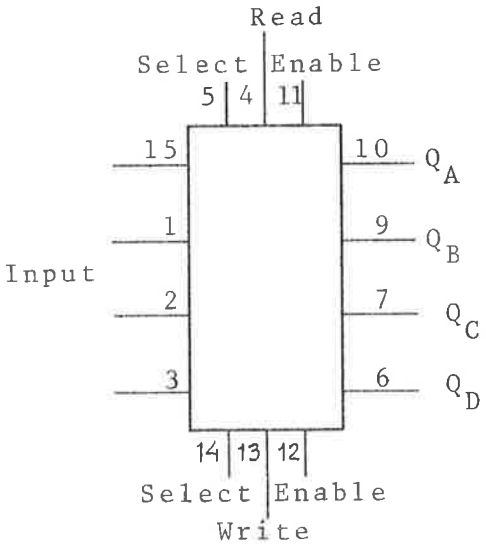
74165
8-bit shift register



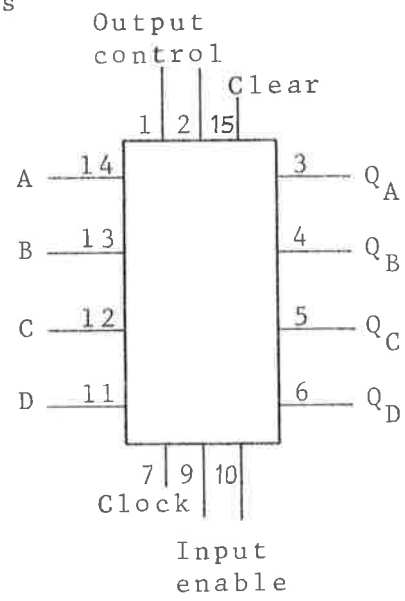
74166
8-bit shift register



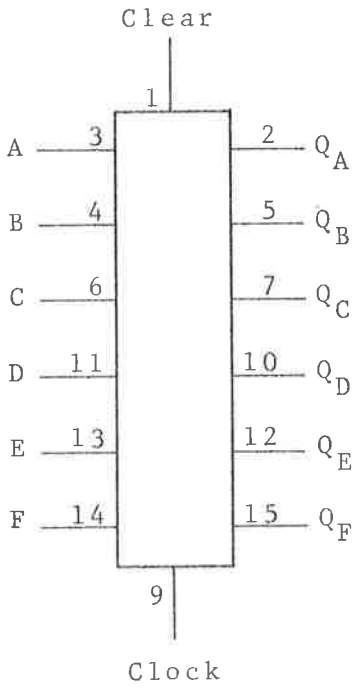
74170
4-by-4 register file



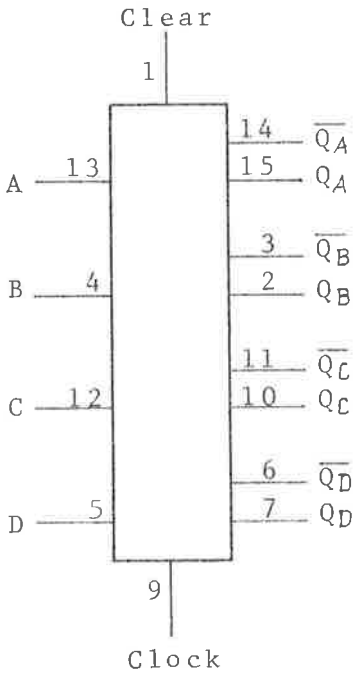
74173
4-bit D-type register with
tri-state outputs



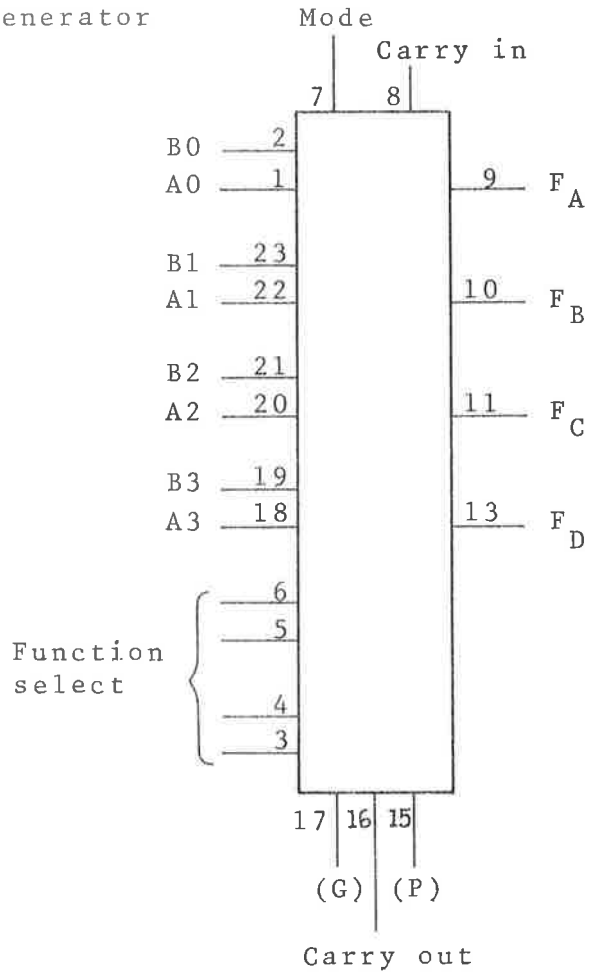
74174
Hex D-flip-flop



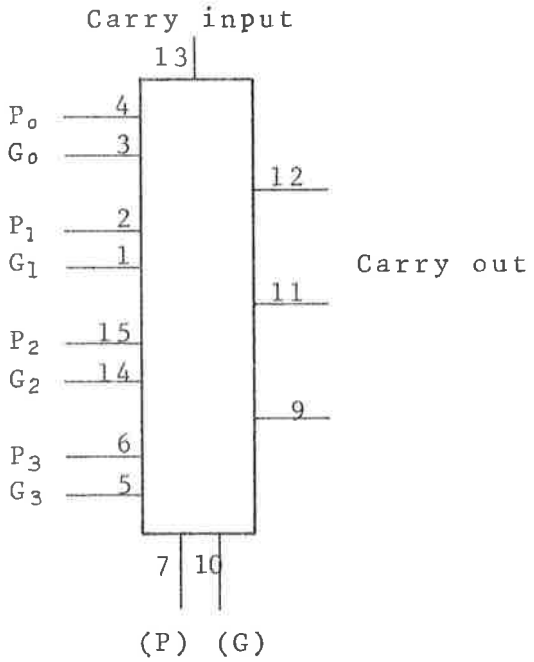
74175
Quadruple D-type flip-flop
with clear



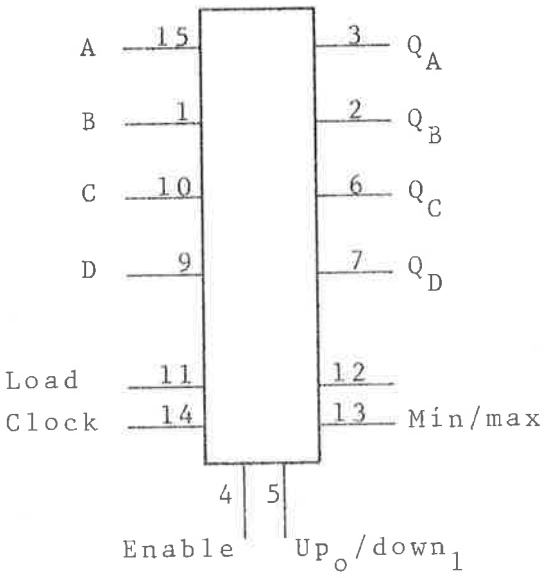
74181
Arithmetic logic unit/
function generator



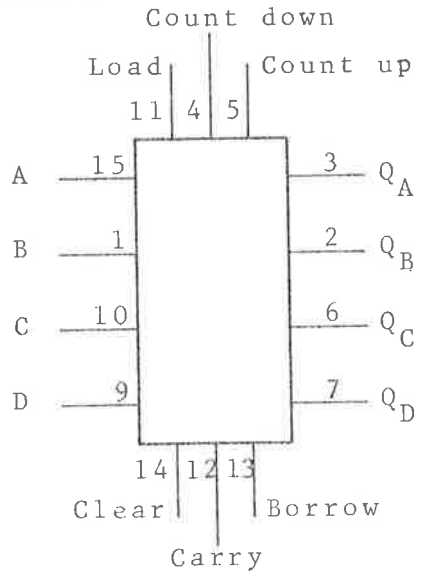
74182
Look-ahead carry generator



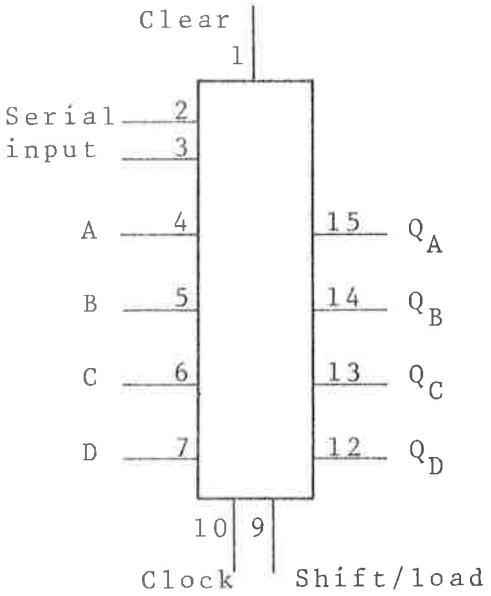
74191
Synchronous up/down counter



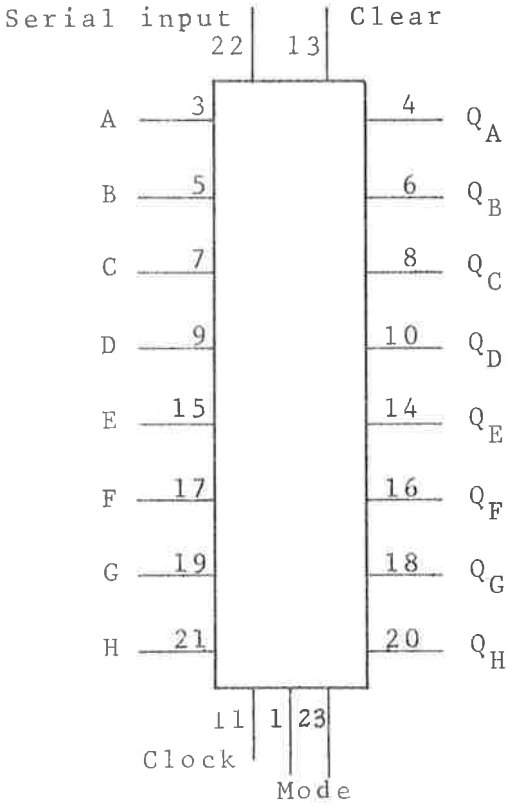
74193
Up/down binary counter



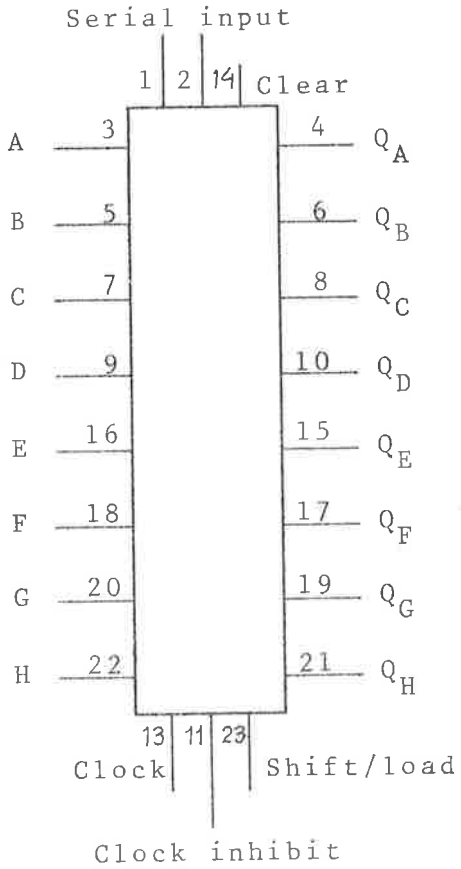
74195
4-bit parallel-access shift register



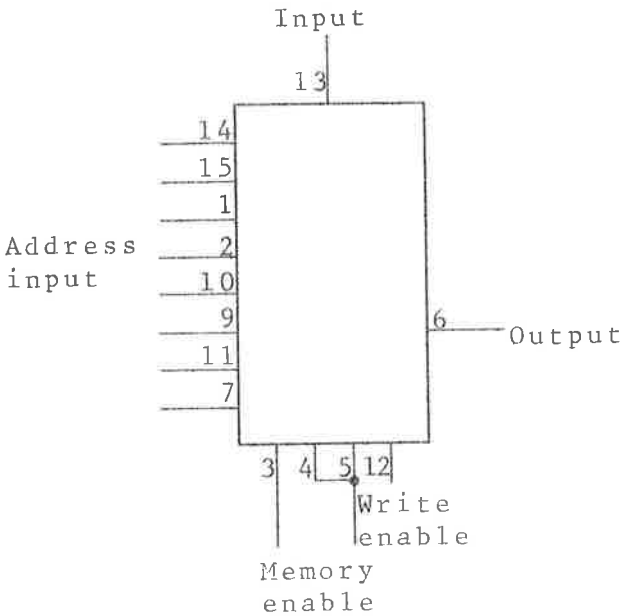
74198
8-bit shift register



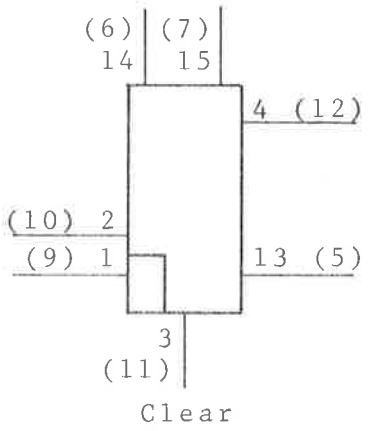
74199
8-bit shift register



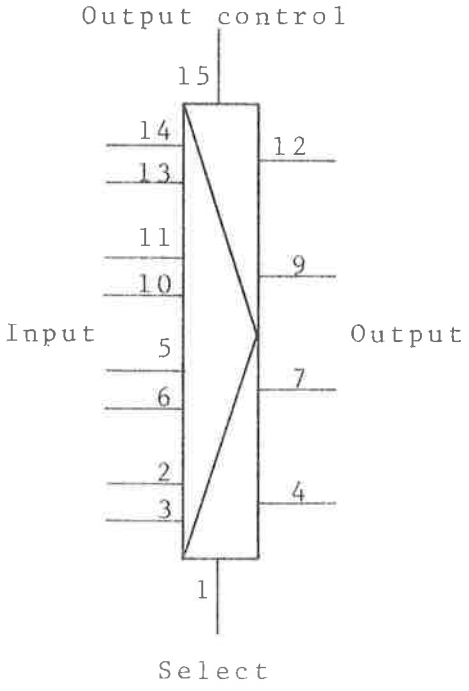
74200
256 bit RAM



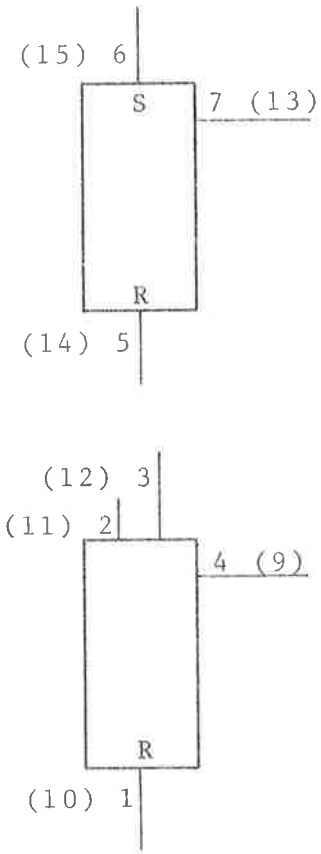
74221
Dual monostable multivibrator
(Pin compatible with 74123)



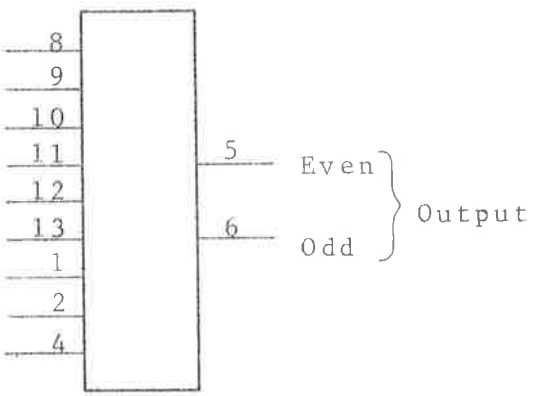
74S258
Quadruple 2-line-to-1-line data selector multiplexer with tri-state outputs



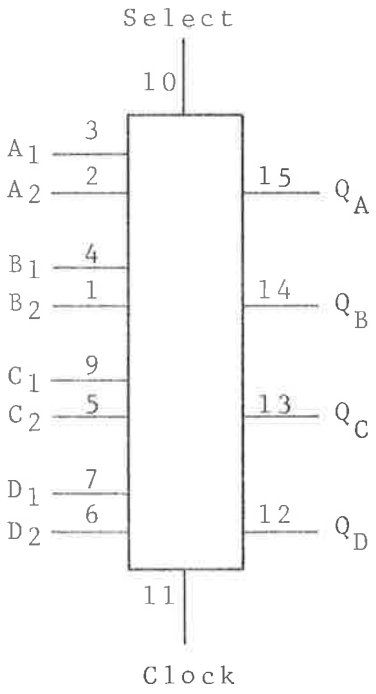
74279
Quadruple S-R latches



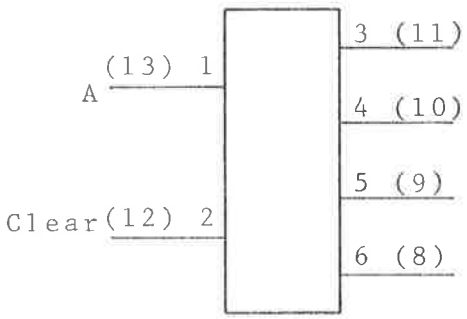
74S280
9-bit odd/even parity generator/checker



74298
Quadruple 2-input multiplexer with storage

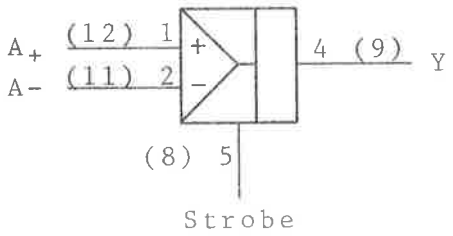


74393
Dual 4-bit binary ripple counter

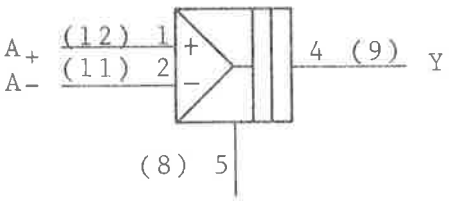


DUAL LINE RECEIVERS AND DRIVERS

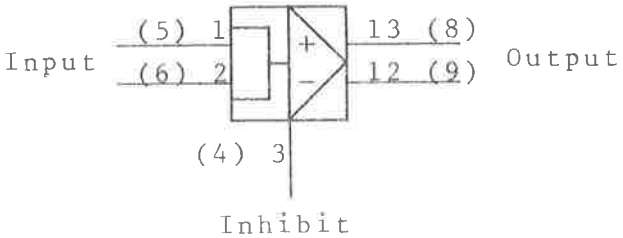
75107



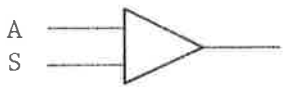
75108 (open collector)



75109-75110

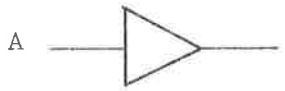


75150
2-input line driver



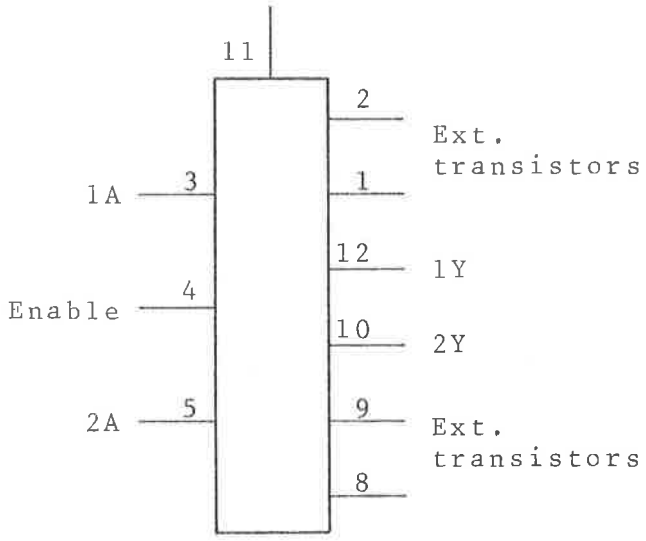
$Y = \overline{A \cdot S}$

75154
Line driver



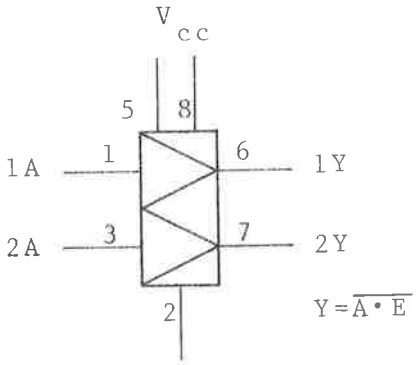
$Y = \overline{A}$

75322
TTL to MOS driver

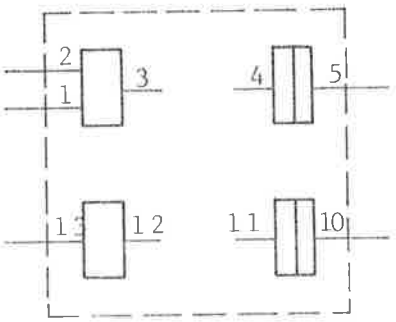


$Y = A \cdot E$

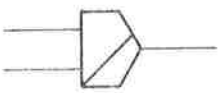
75361
MOS driver



75450
Dual peripheral driver

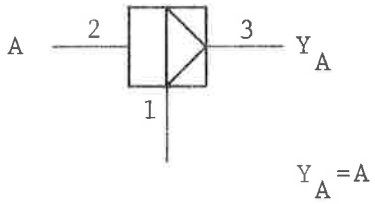


75452B
Dual peripheral driver

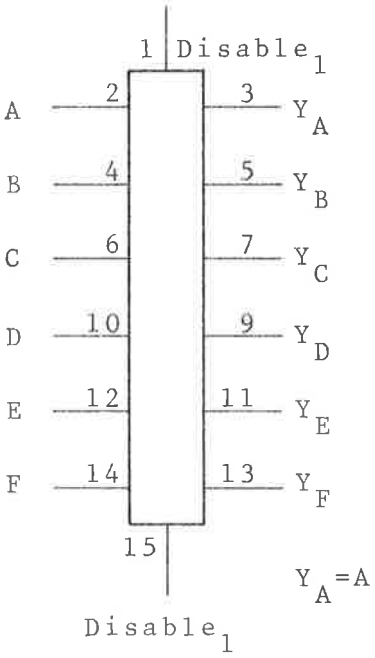


SYMBOLS FOR NSC SERIES DM CIRCUITS

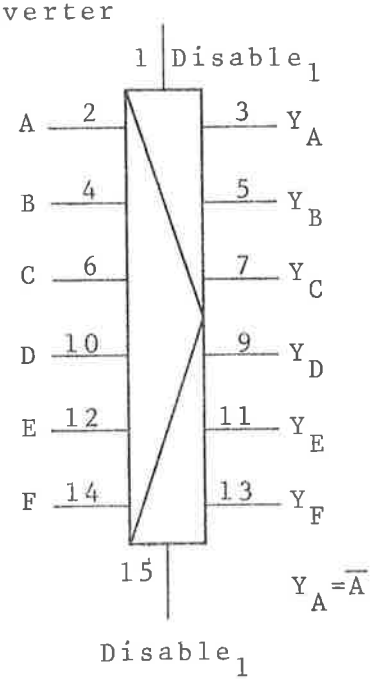
8093
Tri-state quad buffer



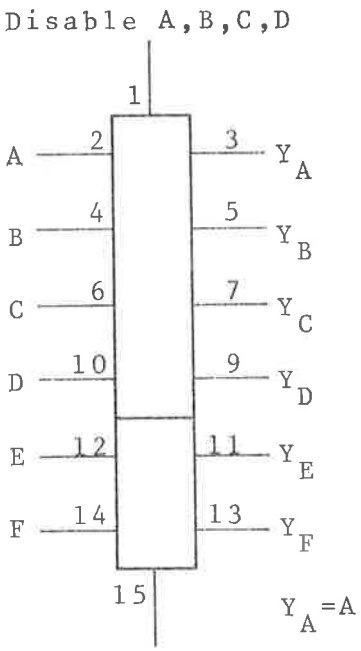
8095
Tri-state hex buffer

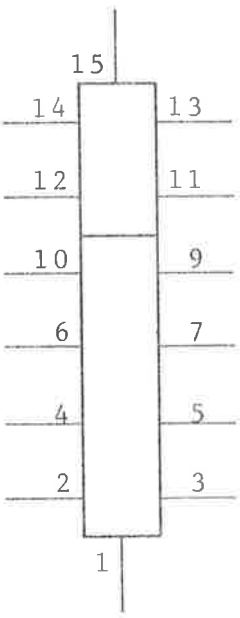


8096
Tri-state hex inverter

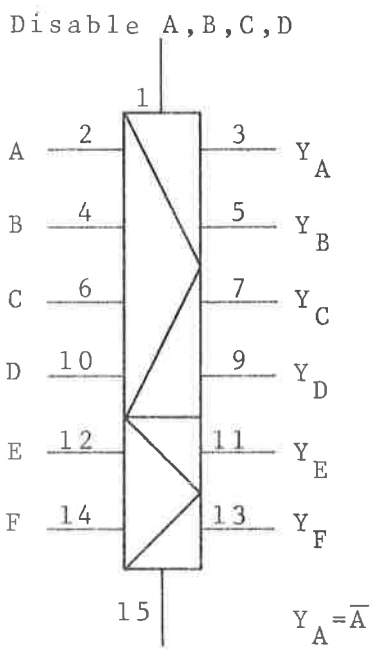


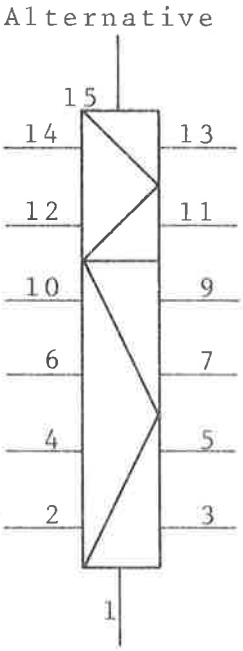
8097
Tri-state hex buffer





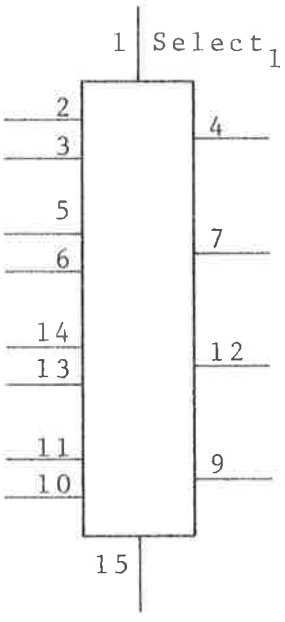
8098
Tri-state hex inverter





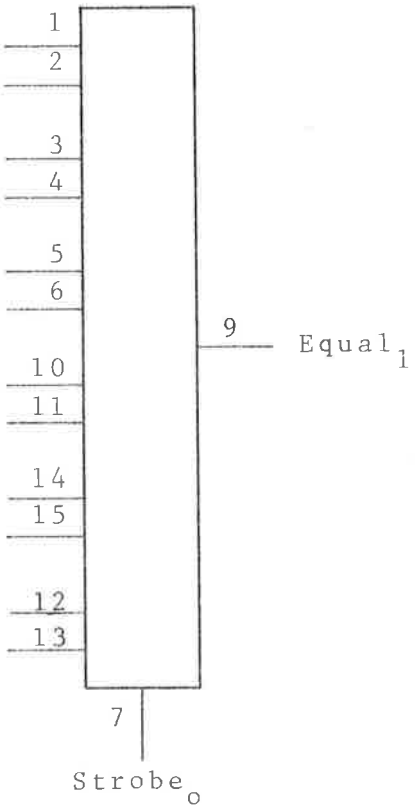
Disable E,F

8123
Tri-state quad 2-input multiplexer

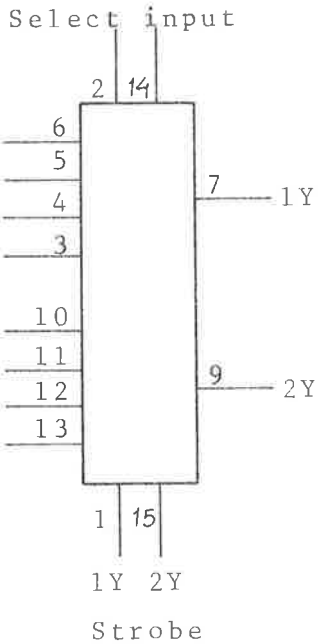


Enable output o

8160
6-bit comparator



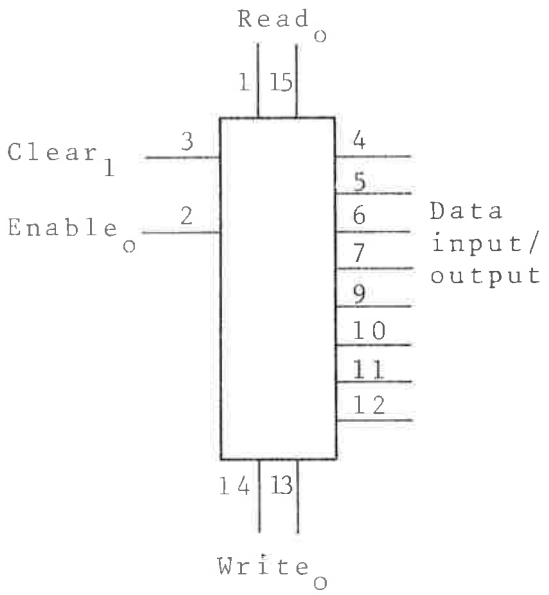
8214
Tri-state dual 4:1 multiplexer



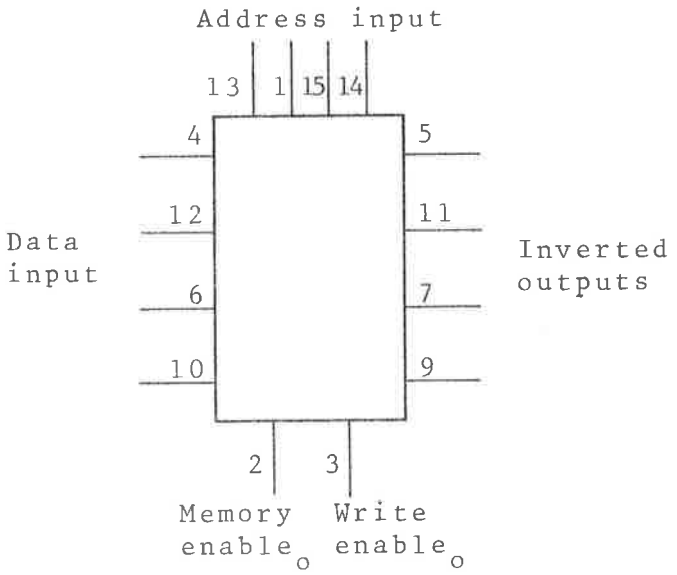
8551
Tri-state quad D flip flop

See 74173!

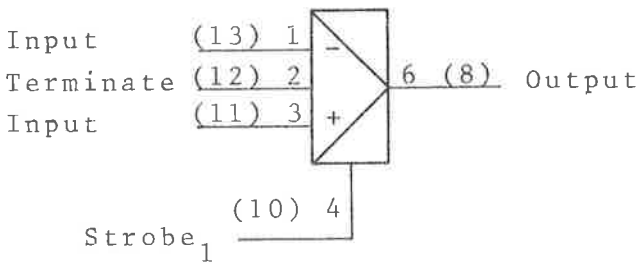
8553
Tri-state 8 bit latch



8599
Tri-state 64-bit random access read/write memory

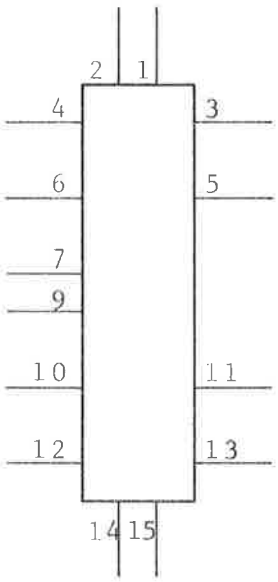


8820
Tri-state line receiver



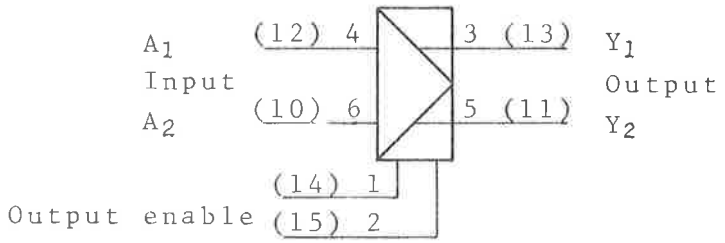
Pins 1 and 2 (13 and 12) are connected when internal termination resistor is used.

8831
Used as single-ended driver



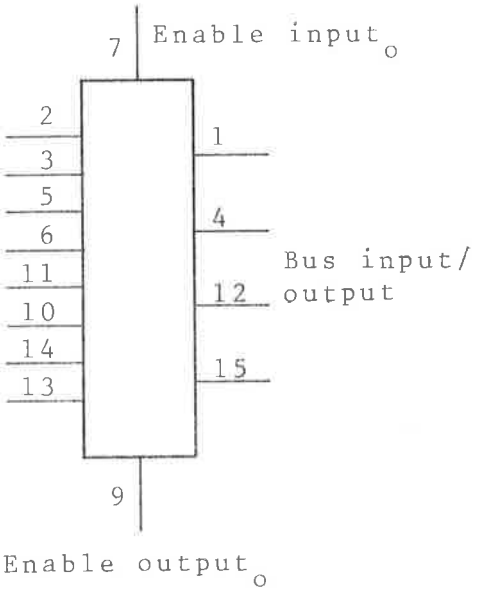
Pins 7 and 9 connected to GND

8831
Used as differential line driver

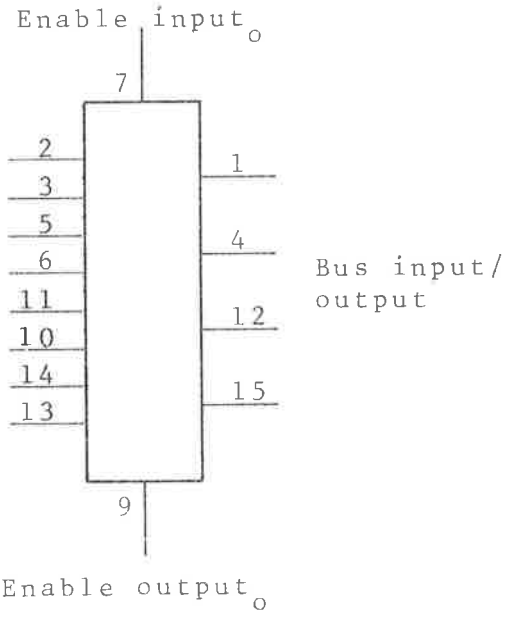


Pins 7 and/or 9 connected to HIGH

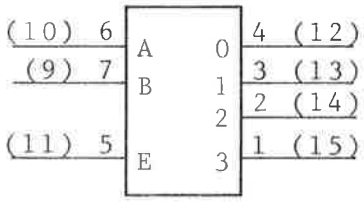
8833
Quad tri-state transceiver



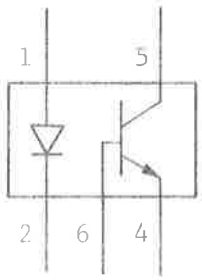
8835
Quad tri-state transceiver, inverting



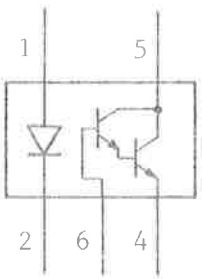
MC 4007
Dual 1-of-4 decoder



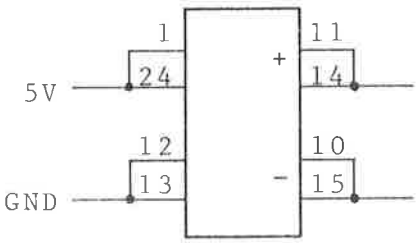
MCT 2
Photo transistor coupler



TIL 113
Photo darlington coupler

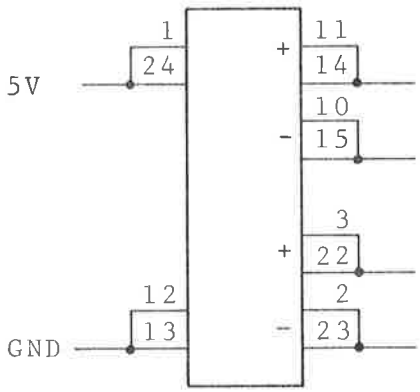


VP 5
Voltage converter

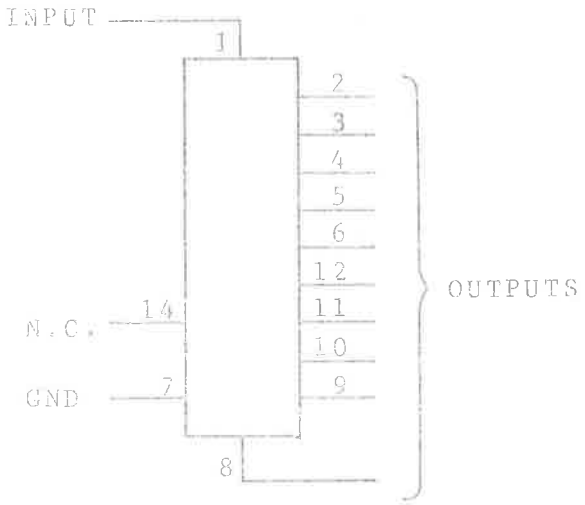


VP 12 is equal to VP 5

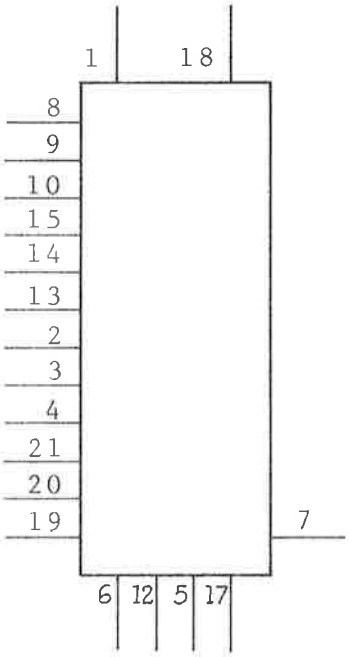
VP 12/12
Voltage converter



DC 10-35T
100 ns delay line with 10 ns taps

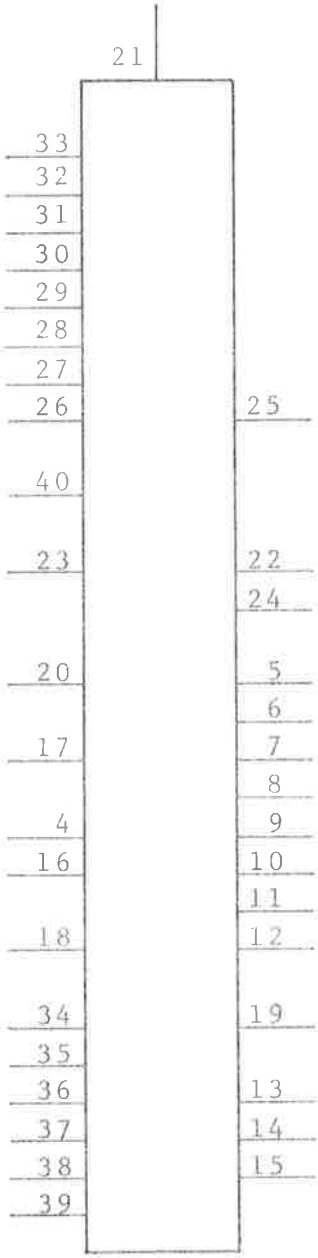


TMS 4030
4 K MOS RAM

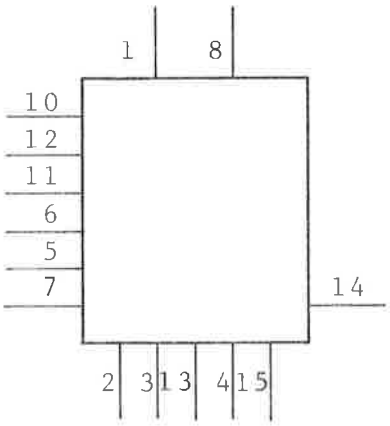


+5V: 11
GND: 22

TMS 6010 (TMS 6011 - AY-5-1012 - AY-5-1013)
Universal asynchronous receiver/transmitter

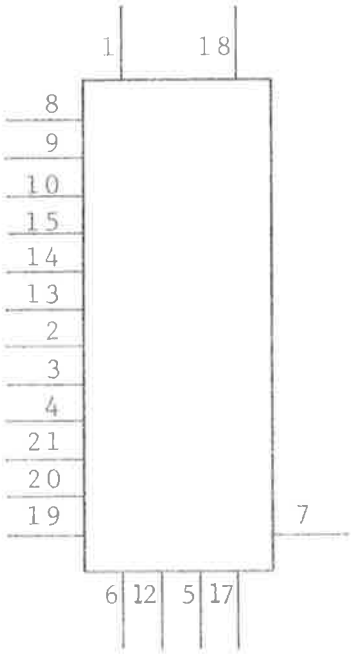


MK 4096P
4 K dynamic RAM 16 pin package



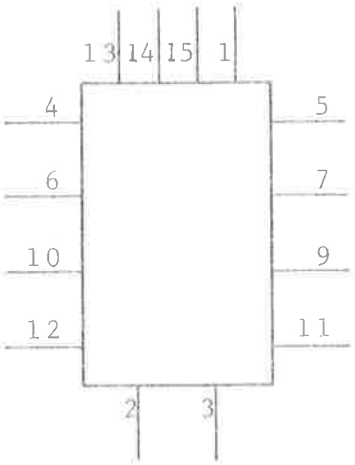
INTEL

2107 B
4 K dynamic RAM 22 pin package



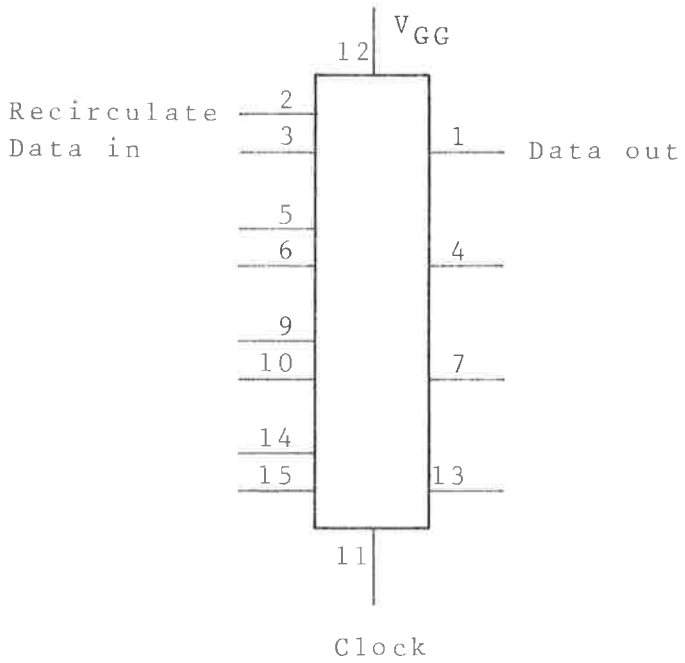
+5V: 11
GND: 22

3101 (Equal to 7489)
64-bit read/write memory



SIGNETICS

2532
Quad 80-bit static shift register



A/S NORSK DATA-ELEKTRONIKK
Lørenveien 57, Oslo 5 - Tlf. 21 73 71

COMMENT AND EVALUATION SHEET

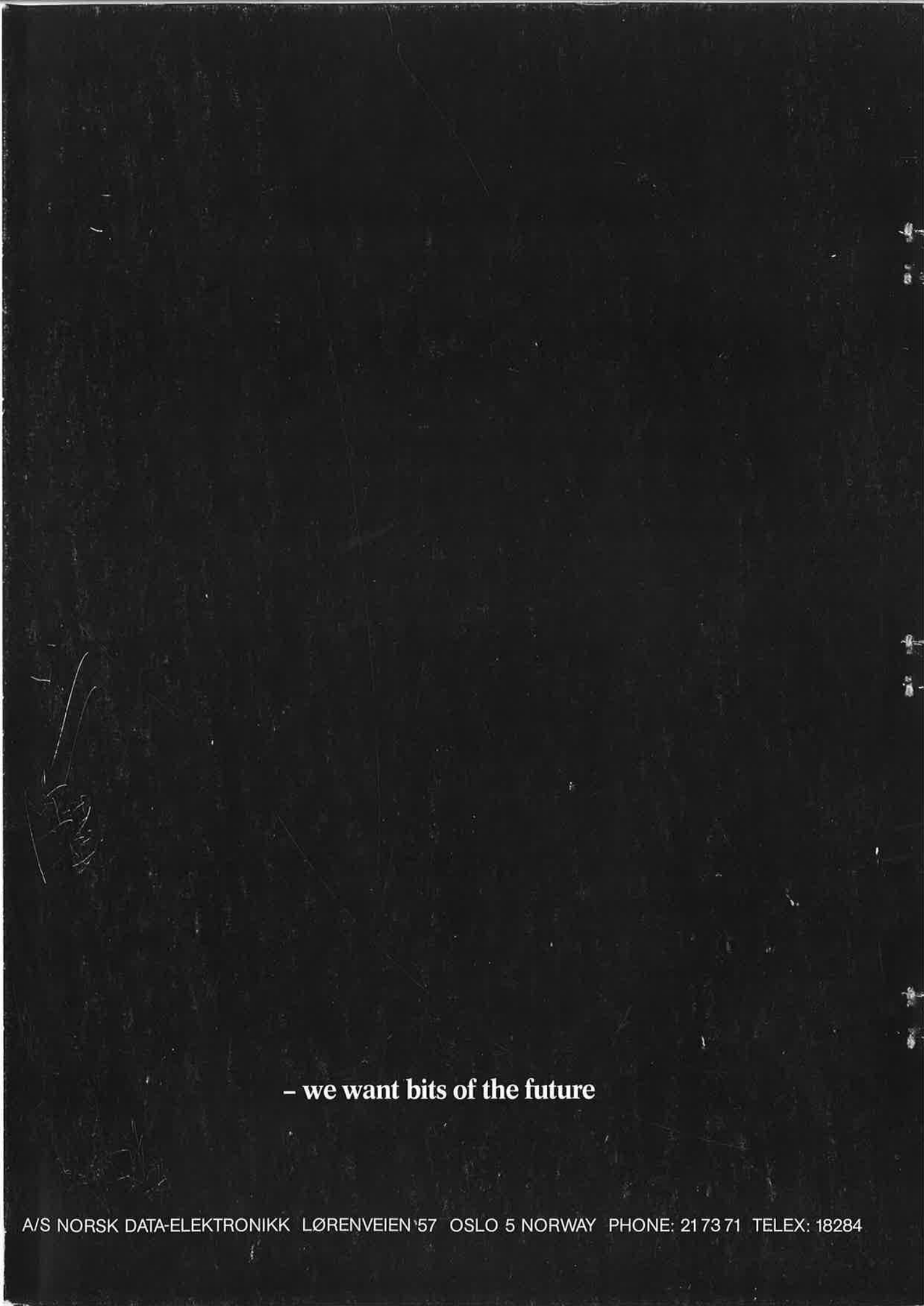
ND-13.003 01 CIRCUIT DIAGRAM SYMBOLS

In order for this manual to develop to the point where it best suits your needs, we must have your comments, corrections, suggestions for additions, etc. Please write down your comments on this pre-addressed form and post it. Please be specific wherever possible.

FROM: _____

_____

_____


– we want bits of the future
A/S NORSK DATA-ELEKTRONIKK LØRENVEIEN 57 OSLO 5 NORWAY PHONE: 21 73 71 TELEX: 18284