# CAMAC

# CC-NORD-10

# (CAMAC CRATE - NORD-10 INTERFACE)

## General Information

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## SUMMARY

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This document describes the operation of the CC-NORD-10 crate controller designed to interface CAMAC crates directly to the input/output bus of the NORD-10 computer.

The CC-NORD-10 contains basic control logic for programmed control of CAMAC commands as well as servicing of LAM requests from CAMAC modules.

Optionally the CC-NORD-10 forms part of a single crate MULTI-CONTROLLER System which has DMA and autonomous program capability. These additional functions are provided by separate controller modules connected to the CC-NORD-10 on a front panel LINK BUS.


References:

| | |
|---|---|
| CC-NORD-10 | - Hardware |
| CC-NORD-10 | - Service |
| CDMA NORD-10 | - General Information |
| CDMA NORD-10 | - Hardware |


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# 1 INTRODUCTION

The CC-NORD-10 is a CAMAC crate controller, conforming to mandatory requirements of ESONE-CAMAC specification EUR 4100 (1972), which interfaces normal CAMAC modules occupying a standard CAMAC crate directly to the Input/Output Bus (IOB) of the NORD-10 computer to be used in the CERN-SPS control system.

The CC-NORD-10 is part of a modular MULTI-CONTROLLER system which can provide the following facilities in each CAMAC crate.

1) Execution of CAMAC read, write and control commands under program control.

2) Efficient real time handling of LAM requests from CAMAC modules using an interrupt vector generator and automasking technique.

3) Control of DMA transfers acting independently of any other CAMAC operations and interleaved with other DMA channels on the NORD-10 IOB.

4) Control of autonomous CAMAC program sequences permitting parallel operation for real time applications of several CAMAC crates without computer control.

The basic program and interrupt controller, CC-NORD-10, which is the subject of this document will be provided in each CAMAC crate. DMA and autonomous function controllers will be added as additional CAMAC modules only where they provide a solution to real time control and data transfer problems.

The design of the CC-NORD-10 has allowed many of the most powerful features of the asynchronous NORD-10 IOB to be extended directly to each CAMAC crate with an easily understandable software addressing format.

1) Addressing of up to 16 CAMAC crates uses the same address structure as standard NORD-10 peripheral devices.

2) All registers except DMA data registers in the CC-NORD-10 may be overwritten and read back for diagnostic purposes at IOB level.

3) CAMAC read, write and control commands can be executed in only one IOB cycle. Dataway status can be read back after each CAMAC command, but this is not often necessary because an automatic check of dataway Q and/or X response can be programmed. Failure to produce an affirmative response can cause an error interrupt.

4) Powerful real time interrupt handling searches for an interrupt source, generates a specific vector corresponding to the highest priority CAMAC LAM request and automasks that source in one IOB cycle

5) Each CAMAC crate may be dynamically programmed to one of three interrupt levels. In addition all crates have access to a fourth high priority interrupt line to service CAMAC errors or urgent real time interrupts from external equipment.

# 2 GENERAL DESCRIPTION

1) Physically the CC-NORD-10 is a two width CAMAC module occupying the two right most positions (control station + 1 normal station) of a standard CAMAC crate.

2) The front panel is shown in Figure 2.1. Connection to the NORD-10 input/output bus (IOB) is via two EMIHUS 88 way connectors. The external IOB must be terminated at the last CAMAC crate on the bus with a passive resistive termination connected to the IOB output socket.

3) The front panel is provided with a CANNON plug (2DB52P) for entry of the LINKBUS which permits optional connection of autonomous and DMA controllers.

4) Four LED indicator lamps provide one shot display of specific controller functions.

5) A maximum of 16 crates may be connected to and addressed by one NORD-10. The logical crate address may be displayed in a reserved space on the front panel.

6) A Lemo socket RA 00-50 C allows connection of one external interrupt of a high priority real time nature.

7) The crate address is physically patched by wire links across a free CANNON socket (2DB 52 S) which plugs into a rear panel mounted CANNON plug (2DB 52 P).

8) The same free socket is used for the LAM grading facility in which the 24 L lines are mixed and patched to form a pattern of 16 graded LAMS.

9) Crate address selection and LAM grading facilities may be more conveniently provided in a separate CAMAC module connected at the rear to the CC-NORD-10 by a short cable. The CANNON socket pin allocation is compatible with the LAM grader socket in ESONE specification EUR 4600.

10) A LEMO front panel socket allows external equipment to generate I on the dataway inhibit bus line in addition to programmed I control.

11) CC-NORD-10 circuitry is contained on two high density printed circuit boards.*) Judicious layout of logic minimizes the number of between board connections. For test purposes the controller can be operated on two CAMAC extender units. Under these conditions the following provisions are made:

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*) Use of arithmetic logic units (ALU) has reduced the total number of integrated circuit packages needed.

a) The card at the control station can be hinged to 90 $^{o}$ for circuit inspection. This implies the use of a flexible module extender such as TEKDATA type 1030.

b) Clearly marked oscilloscope test points are provided on the card for dataway bus lines S1, S2, B.

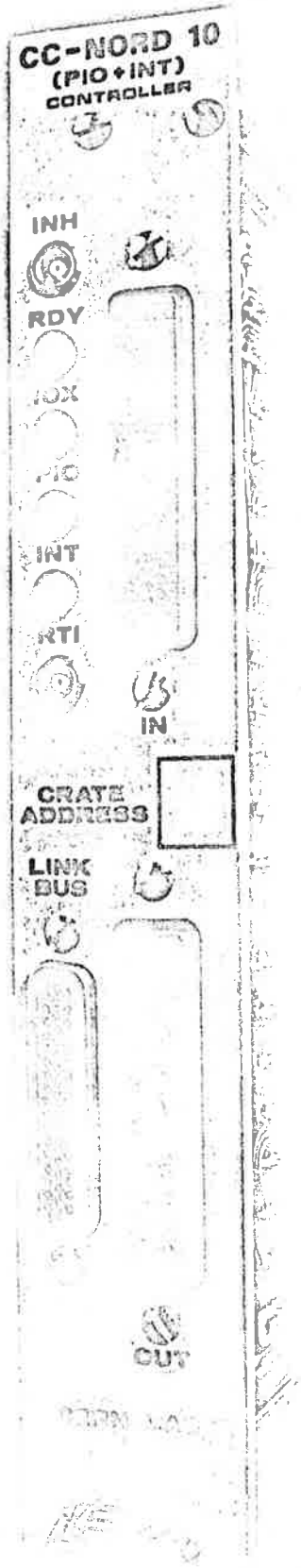

CC-NORD 10
(PIO+INT)
CONTROLLER
INH
RDY
IOX
PIO
INT
RTI
IN
CRATE ADDRESS
LINK BUS
CUT

Figure 2.1

# 3 SPECIFICATIONS

The following paragraphs list in detail the specifications for the CC-NORD-10 programmed input/output (PIO) and interrupt (INT) controller. Brief details of the NORD-10 input/output bus (IOB) structure are given where they are important to the understanding of the CAMAC interface. In addition a specification is given for the LINK-BUS which allows the addition of DMA and autonomous controller options forming part of the modular multicontroller system outlined in report CERN LAB II-CO/73-1.

## 3.1 Physical and Electrical Specifications

1) A general description has been given in Chapter 2. All mechanical aspects of the CC-NORD-10 comply with standard CAMAC dimensions referred to in Chapter 4 of ESONE specification EUR 4100 (1972).

2) The controller uses the standard CAMAC power bus line +6V. No other power lines are used. Maximum power dissipation and current ratings are observed, but because power dissipation exceeds 8 W per station, a CAMAC crate with forced ventilation must be used.

3) The controller makes use of the standard contact allocation for connectors at the control and normal stations on the CAMAC dataway.

4) The CC-NORD-10 has 16 bit data transfer capability between CAMAC read/write lines and the 16 data lines of the NORD-10 IOB. Dataway lines W17 - 24 and R17 - 24 are not used but pull up current sources are provided at the controller. Normal modules with 24 bit capability may only be operated in 16 bit mode. In cases where higher than 16 bit precision is called for, 32 bit precision can be obtained with two successive 16 bit transfers.

## 3.2 NORD-10 External IOB to CAMAC

A detailed description of the NORD-10 IOB is contained in the NORD-10 I/O Manual, March 1973. The external IOB from the NORD-10 meets the specific demands of CAMAC and includes the following data, address and control lines:

| No. of Lines | Name | Function | Source | |
|---|---|---|---|---|
| | | | CPU | CAMAC |
| 16 | DATA | Read/write data | 16 | 16 |
| 16 | ADDRESS | CC-NORD-10 register address or core address for (DMA) | 11 | 16 |
| 1 | IOXE | IOX enable | 1 | - |
| 1 | CONNECT | CC-NORD-10 ready | - | 1 |
| 4 | INTERRUPT | Interrupt request lines | - | 4 |
| 1 | IN/OUT IDENT | Interrupt search | 1 | 1 |
| 1 | IN/OUT GRANT | DMA search | 1 | 1 |
| 1 | INPUT | Data direction { I = INPUT, O = OUTPUT } | - | 1 |
| 1 | DMA REQUEST | Request IOB for DMA Xfer | - | 1 |
| 1 | DMA DATA READY | Data ready/received at CPU for output/input DMA | 1 | - |
| 1 | MASTER CLEAR | Clears CC-NORD-10 registers (generates CAMAC Z) | 1 | - |
| Total 44 | | | | |

Figure 3.1

The external IOB from the NORD-10 to CAMAC crates is supplied on 44 twisted pair cable terminated with 88 way EMIHUS connectors. Up to 16 CC-NORD-10 CAMAC crate controllers may be interconnected on the IOB.

Interrupt and DMA requests from each CC-NORD-10 are ORed on to the request lines using tristate line drivers in either 1 state or disabled as several sources may operate these lines simultaneously as shown.

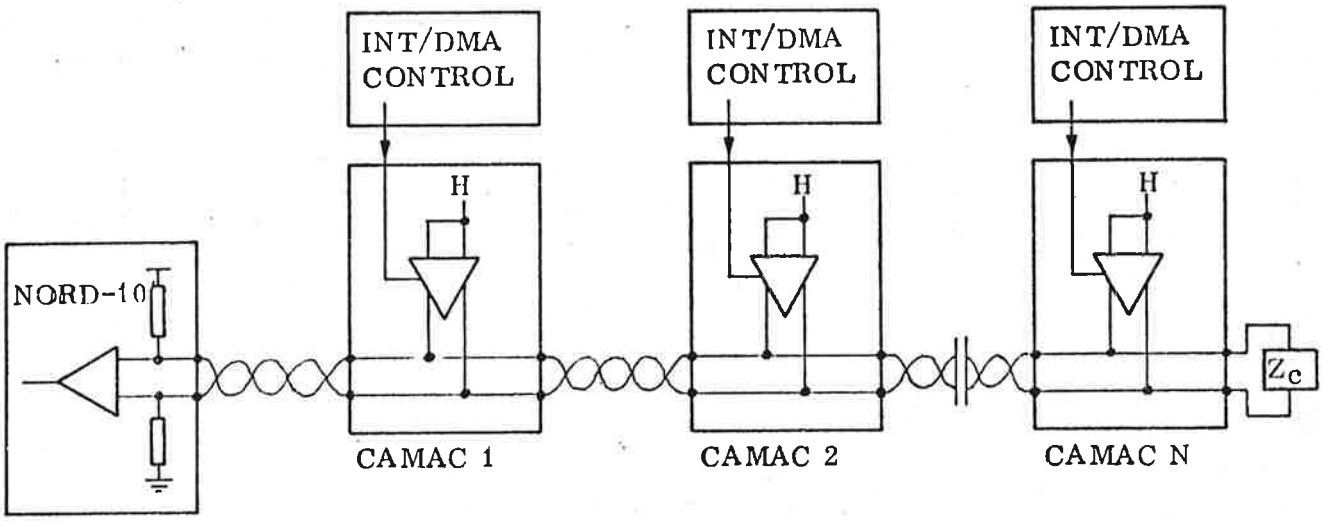



Figure 3.2

All other lines are operated with tristate logic signals using a balanced line driver and terminating receiver combination in each case. Data and address lines are operated in a bidirectional mode as shown.

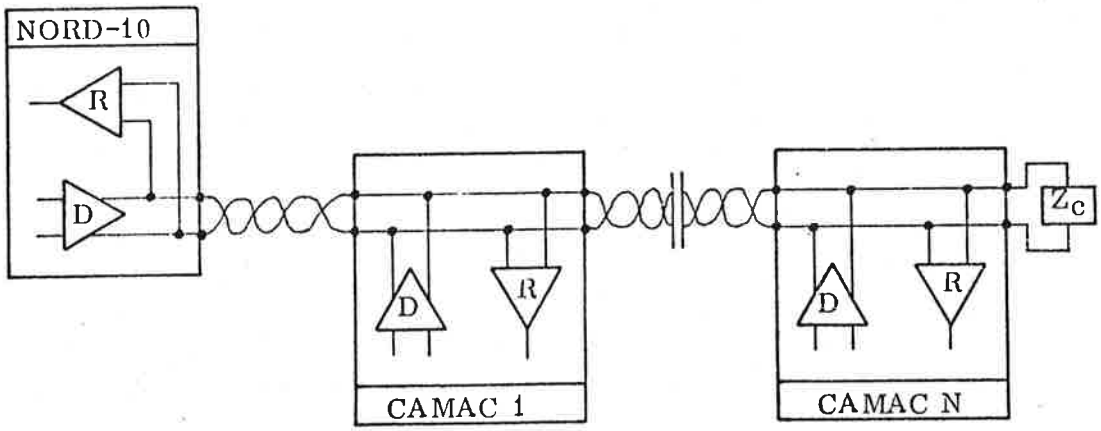



Figure 3.3

Bidirectional transmission on some IOB lines does not permit common mode noise rejection greater than ± 15 V. For this reason the external IOB length may be arbitrarily limited in noisy environments. In addition all CAMAC crates connected to the external NORD-10 IOB must be powered from the same mains supply as the NORD-10 computer and careful attention must be paid to the physical layout of interconnecting earth circuits in such environments.

The tristate line driver/receiver technique permits high speed transmission of terminated IOB signals over very long bus lengths as well as rejection of induced noise signals over a wide bandwidth on individual twisted pair lines.

No provision has been made for allowing CAMAC crates connected to the IOB to be 'OFF LINE' whilst other CAMAC crates on the IOB are operational. In this respect it is impossible to prevent IOB data corruption during the transitional states from ON to OFF LINE or vice versa. For this reason all CAMAC crate controllers physically connected to the IOB must be powered before any part of the CAMAC system can be operational.

## 3.3 CAMAC Operations under Program Control

Programmed operations (PIO) between the NORD-10 and the CAMAC crate controller use the IOX instruction which controls all operations to peripherals on the NORD-10 IOB. Unless otherwise specified these operations involve data transfer between the CPU A register (A reg.) and a specified register in an addressed peripheral device such as a CC-NORD-10 CAMAC crate controller.

The PIO section of the CC-NORD-10 contains three addressable registers for executing CAMAC commands.

1) Control and Status register

2) Data register

3) NAF register

The addressing and data format for each of these registers at a specified CAMAC crate are shown in Appendix A. Typical program sequences for CAMAC commands are shown in Appendix B.

Execute NAF or DATA is used to generate a CAMAC dataway cycle under program control. The content of the NAF register, bits 3, 4 corresponding to CAMAC function lines F8, F16 are sensed as follows to determine whether a CAMAC read, write or control command must be executed.

| | |
|---|---|
| READ COMMAND | if $\overline{F8}.\overline{F16} = 1$ |
| WRITE COMMAND | if $F8.\overline{F16} = 1$ |
| CONTROL COMMAND | if $F8.\overline{F16} + F8.F16 = 1$ |

This logic is also used to determine the direction of data flow from the DATA register and subsequently on the IOB data lines.

CAMAC WRITE commands consist of two IOX instructions. Either data is first stored in the DATA register before loading the NAF register and executing the dataway cycle, or the NAF data is first stored in the NAF register before loading the DATA register and executing the dataway cycle. In both cases the contents of the data register are put on the dataway write lines. If more than one write cycle is wanted with constant NAF register or constant DATA register, only one IOX instruction is needed for each additional dataway cycle.

For CAMAC READ commands the NAF register is loaded, the dataway cycle is executed and the DATA register is used to store read line data at S1 until it is strobed into the A register. This read operation is completed in one IOX cycle.

For CAMAC CONTROL commands the data register remains unchanged.

Special use is made of the NAF register for the CAMAC UNADDRESSED commands Initialize (Z) and Clear (C). During both these operations data in the NAF register and DATA register are cleared.

After each dataway cycle the status register may be read in a further IOX cycle to inspect dataway Q, X response etc., from the previous dataway operation.

The control register can be overwritten to define various CC-NORD-10 interrupt control modes. Again the status register may be used to inspect status of interrupt flags as well as to check control bits. Data content of each of the specified registers may be verified using the apparently redundant IOX read instructions shown in the addressing format. These functions can be used in diagnostics to check the continuity of the IOB from the NORD-10 to the most distant CAMAC crate.

## 3.4 Computer Interfacing under Interrupt Control

The following sections describe the interrupt handling logic for normal LAM requests provided at each CAMAC crate by the interrupt section (INT) of the CC-NORD-10. This logic is controlled by a programmable MASK register together with specific bits in the CONTROL register. The relevant addressing and data formats for these registers at a specific CAMAC crate are shown in Appendix A. Appendix B shows typical IOX instructions which can be used for interrupt service operations.

### 3.4.1 Interrupt Handling (NORD-10 IOB)

This section should be read in conjunction with Section 7.1 of the NORD-10 I/O Manual.

1) The interrupting CAMAC crate places its demand on the INTERRUPT LEVEL LINE to which it is set by programmed control of respective bits in the CC-NORD-10 CONTROL register.

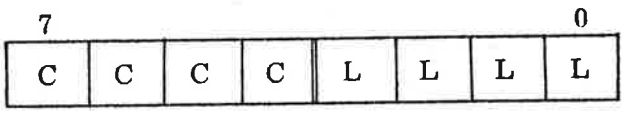
2) In response to the special IOX IDENT instruction, INIDENT is generated at the CPU and received by the first CAMAC crate.

3) OUTIDENT is transmitted to the next crate if the interrupt is not found at the priority level code set on the ADDRESS lines (Address lines are compared with the interrupt level bits set in the CONTROL register).

4) When the interrupting crate recognizes the INIDENT signal from the previous crate OUTIDENT is not sent to the next crate. Instead CONNECT and INPUT signals are returned to the CPU.

5) CONNECT implies that the INTERRUPT source has been recognized.

6) INPUT implies that the DEVICE IDENTIFICATION NO. (vector address) is static on data lines 0-7. The vector address is unique for each graded LAM in a CAMAC system and has the following data format:




where C is the 4 bit CAMAC crate code and L is the 4 bit GRADED LAM code.

### 3.4.2 Interrupt Controller Specification

The interrupt controller contains the following logic:

1) An external LAM GRADED module provides the possibility for patching 23 'L' lines to 16 GRADED LAM lines within each crate. Up to four 'L' lines may be mixed on to any one graded LAM line. The LAM grader provides additional current if more than one 'L' is patched to any GRADED LAM line.

2) A LAM MASK REGISTER is used to enable (BIT SET) or disable (BIT CLEAR) any one of the 16 graded LAMs. If the demand is disabled, then the L line is maintained by the module LAM source until reset by program control. Reading of LAM STATUS gives the condition of any 'L' line during such periods.

3) A one bit CRATE DEMAND MASK followed by a 3 bit programmeable multiplexer places the inclusive OR of all demands passing through the LAM MASK REGISTER on to the desired IOB INTERRUPT REQUEST LINE.

4) A 16 BIT PRIORITY ENCODER is used to generate a 4 bit binary number corresponding to the highest graded LAM interrupting. This may change until the INPUT signal is issued at CONNECT time.

5) After CONNECT, data must remain static and is stored in a 16 bit register. This register is not released until it has been decoded to a 16 bit word again and used to automatically BIT clear (disable) the appropriate bit of the LAM MASK REGISTER.

3.4.2.1 LAM Handling

1) 23 L lines at the control station are wired to the rear panel connector type CANNON 2DB52S.

2) Mixing and patching of L lines will normally take place in an external LAM GRADER module.

3) 16 graded LAMs are returned on the same 52 way connector. Pin assignment is compatible with the LAM grader connector in ESONE Specification EUR 4600.

3.4.2.2 Priority Vector Generator

The 4 bit binary number corresponding to the highest demand level at CONNECT time is added to the fixed 4 bit crate address and 1 bit defining CAMAC to form the vector address or DEVICE IDENTIFICATION NO. This address is used by the software to point directly to the service subroutine which may cause an inmediate CAMAC operation or set a software flag for later action.

Note that no CAMAC dataway cycle has been executed in determining the vector address itself.

No further interrupt at the same or lower levels may be serviced until the service subroutine terminates.

All interrupt handling operations whether vector addressing or LAM mask operations occur inside one IOX instruction. If a higher level interrupt changes the mask in the same CAMAC crate, then the high level software has the responsibility for reading the LAM mask and restoring to its original condition upon completion. Under these conditions CONTROL/STATUS and DATA registers must also be saved and restored if a CAMAC cycle is generated at the higher level.

### 3.4.3 High Priority immediate Interrupt

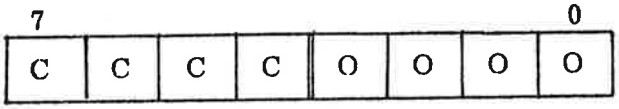
Interrupt level 13 on the NORD-10 IOB has been reserved for the following high priority demands at each CAMAC crate

1) External real time urgent demands.

2) Automatic Q, X error interrupts.

The CONTROL/STATUS register is used to enable, disable or test the status of each source when an interrupt occurs. The data bit format and set/reset characteristics are described in Appendix A.

When interrupt level 13 occurs, the same interrupt operations occur as for normal interrupts but only a 4 bit crate vector is returned so that level 13 service software knows which crate is interrupting.




The exact interrupt source is obtained by inspecting the STATUS register at that crate. The following diagram indicates briefly the logic used for controlling each interrupt source at level 13.

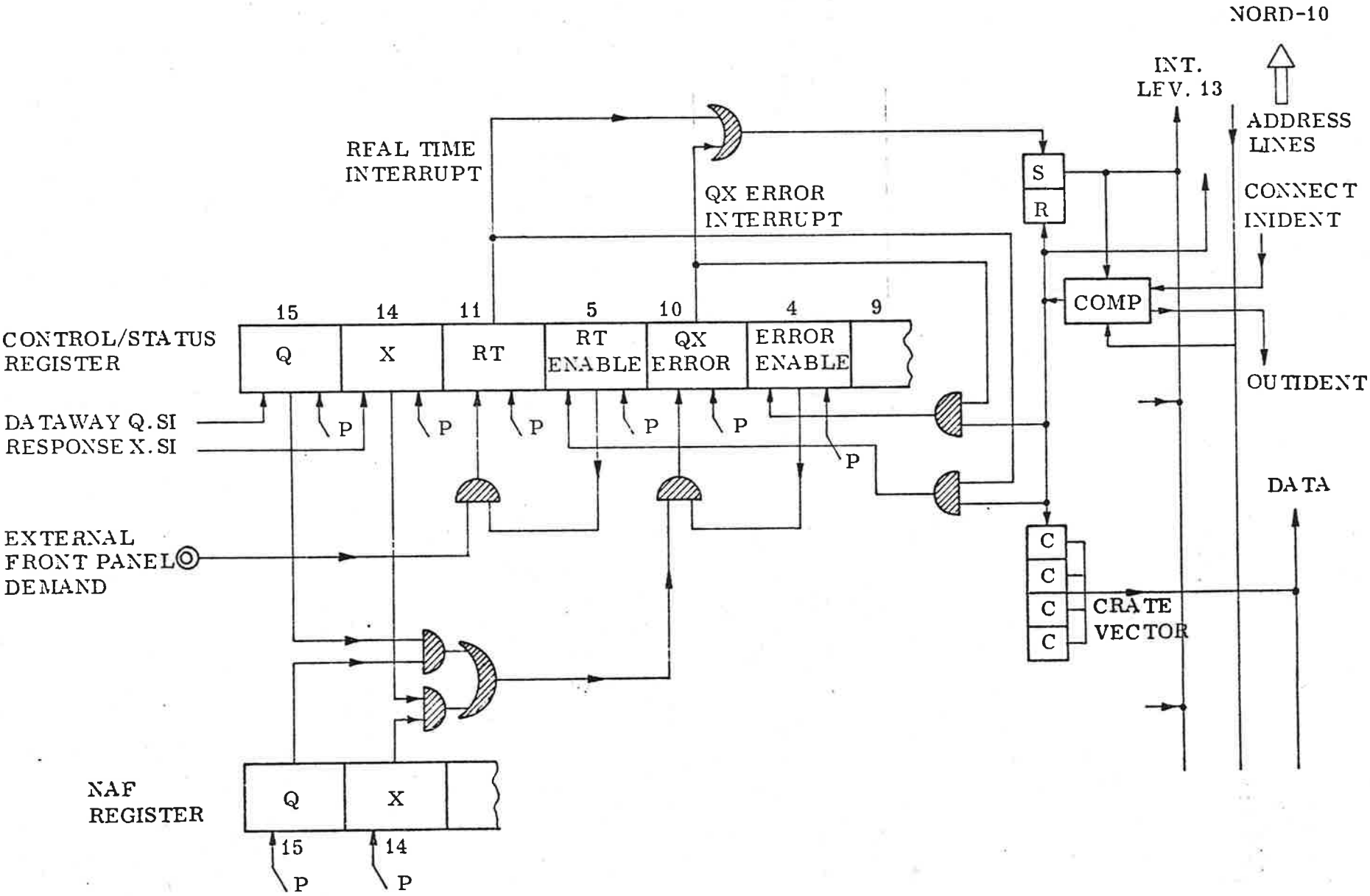

NORD-10
INT.
LEV. 13
ADDRESS
LINES
CONNECT
INIDENT
REAL TIME
INTERRUPT
QX ERROR
INTERRUPT
S
R
COMP
OUTIDENT
15
14
11
5
10
4
9
CONTROL/STATUS
REGISTER
Q
X
RT
RT
ENABLE
QX
ERROR
ERROR
ENABLE
DATAWAY Q.SI
RESPONSE X.SI
P
EXTERNAL
FRONT PANEL
DEMAND
DATA
C
C
C
C
CRATE
VECTOR
NAF
REGISTER
Q
X
15
14
P
P = PROGRAM CONTROL BITS

Figure 3.4

## 3.5 Preparation for Computer Control

This section concerns the initialization of each CAMAC crate. This initialization must be made before program control can commence. Initialization may be necessary for several reasons:

1) Controlled power on from cold start.

2) Controlled power off/on for maintenance purposes.

3) Uncontrolled power off/on due to short term mains failure.

4) Uncontrolled power on after long term mains failure.

5) Master clear following software or IOB lock-out during commissioning.

### 3.5.1 NORD-10 MASTER CLEAR

Under computer cold start conditions MASTER CLEAR resets all logic and clears all registers except MASK register in all CC-NORD-10 controllers. Master clear then generates a CAMAC Initialize (Z) cycle on each CAMAC dataway.

### 3.5.2 Crate Power Up

Power up of each CAMAC crate whether controlled or uncontrolled causes the following sequence of operations.

1) All logic is reset and all registers except MASK register are cleared in the CC-NORD-10 CAMAC crate controller as for NORD-10 MASTER CLEAR.

2) CAMAC dataway Z is then generated and the Z bit set in the status register at time S2 during the dataway cycle.

Uncontrolled power off during normal operation will result in an external IOB timeout and interrupt on level 14.

Dataway Patch pin P1 at the control station is used for communication between power supply and the CC-NORD-10. When power is turned on, P1 carries a low level signal, and the end of this is used to generate the controller clear and dataway Z signals.

In the operational environment of unmanned auxiliary buildings it would be impractical to provide POWER ON logic which requires manual re-setting to ON LINE status after a POWER TRIP.

It seems clear that several software actions will result corresponding to the sequences specified at the start of this section.

Software tasks cannot commence until the whole CAMAC system has ON LINE status. If controlled power off/on is required for maintenance, then software should ensure that tasks using CAMAC cannot be started. It is clear that the CAMAC system cannot be dedicated for maintenance until current tasks using CAMAC have been completed.

Uncontrolled POWER TRIP on any CAMAC crate will give rise to several actions:

1) A current CAMAC command will TIME OUT.

2) All active tasks must be completely restarted when power returns even if no CAMAC command was currently being executed, because all LAM sources will be cleared and disabled by the POWER ON Z cycle.

3) No further tasks may be started until power is returned to offending CAMAC crates and the whole system again has ON LINE status.

4) If power failure is of a temporary nature, then software monitoring ON LINE status can automatically restart waiting tasks. Longer term power failure requires a different strategy if important tasks cannot be completed within their allocated time.

### 3.5.3 Generation of Dataway Control Signals Z, C, I

Figure 3. shows the various ways in which Z, C and I dataway signals may be generated. Three operations may generate Z.

1) CRATE POWER UP
2) PROGRAMMED COMMAND (See Appendix A)
3) NORD-10 MASTER CLEAR

The CC-NORD-10 provides the following mandatory actions:

1) Z is generated by the controller and used by module at time S2.

2) Dataway BUSY (B) is generated.

3) C is generated and used by module at time S2.

4) I = 1 is generated. I is maintained in this condition until specifically reset.

5) S2 and S1 are generated at the correct times during the dataway cycle.

After the execution of Z for any reason the status of the dataway Z line at time S1 is strobed into status register bit 13. For this reason resetting of crate controller logic, if necessary, always precedes execution of an unaddressed dataway cycle generating Z or C.

Dataway Clear (C) is generated during a Z cycle or under program control (see Appendix A).

Under this command an unaddressed dataway cycle is initiated. The state of the C bus line is strobed into bit 12 of the status register at time S1.

Dataway INHIBIT (I) can be set by four separate actions:

1) By Z cycle.
2) Program control (see Appendix A).
3) External signal via front panel LEMO socket.
4) Another control module which has capability of generating I on the dataway.

INHIBIT may be reset by:

1) Program control.
2) Removal of external signal.
3) Removal of I at alternative control module.

It is clear that I status may change at any time. Status register bit 0 monitors the state of the dataway I line directly and is the inclusive OR of all I sources.

## 3.6 Multicontroller Operation

The multicontroller concept allows for varying degrees of control within the CAMAC crate depending upon the application. Basically, program and interrupt control are provided in the CC-NORD-10 interfacing to the NORD-10 external IOB. The CC-NORD-10 therefore provides the basis for all forms of control. In addition DMA or autonomous (AFC) function controllers may be added which use the CC-NORD-10 either to request an IOB cycle for NORD-10 memory access and/or to obtain control of the dataway for one CAMAC cycle.

The AFC and DMA controllers consist of single width CAMAC modules whose control, address and data registers may be set via the dataway using the CC-NORD-10 in program mode as for normal CAMAC modules. When DMA or AFC control has been enabled, each control cycle is requested and granted in real time of the peripheral equipment by means of the front panel LINK BUS which interconnects each of the controller modules. When a specific process has been completed each controller has the capability of generating a LAM request which is handled in the same way as for normal CAMAC modules.

The modular multicontroller concept allows rapid build up of CAMAC control systems to cope with specific real time control or data transfer problems as they arise in individual CAMAC crates. In particular there are minimal system overheads for DMA or AFC control. The addition of an extra CAMAC module and interconnecting cable together with the initializing software are the only prerequisites to provide several DMA and up to two AFC controllers in each CAMAC crate as and when necessary. Furthermore modularity permits interchangeability and independent testing of each part of the control system.

### 3.6.1 LINK BUS Characteristics

The LINK BUS has the capability for connecting several (linked priority) DMA controllers and up to two AFC controllers into the CC-NORD-10 and is carried on a 52 way twisted pair cable terminated with CANNON connectors (type 2DB52S). The following table lists the function of each LINK BUS signal as well as the interfacing standard used.

| LINK BUS SIGNALS | | |
|---|---|---|
| Pin | Function | Signal Standard |
| 1 - 5 | Station address N to control station (25) N1, 2, 4, 8, 16 | TTL |
| 6 | Ground | |
| 7 | Request AFC 1 | TTL |
| 8 | Grant AFC 1 | |
| 9, 10 | Ground | |
| 11 | Request AFC 2 | TTL |
| 12 | Grant AFC 2 | |
| 13 | Request DMA | TTL |
| 14 | Grant DMA (Dataway) | |
| 15 | Grant CPU | |
| 16 | Channel Ready | |
| 17 | Ground | |
| 18 | INPUT (direction of data transfer on IOB) | TTL |
| 19, 20 | DMA memory address BIT 0 | Tristate TSL |
| 33, 34 | Signal - return DMA memory address BIT 7 | |
| 35, 36 | Ground | |
| 37, 38 | DMA memory address BIT 8 | |
| 51, 52 | DMA memory address BIT 15 Signal - return | " |

### 3.6.2 Dataway Grant Logic

The PIO, DMA and AFC controllers each need to generate dataway cycles on the CAMAC dataway. The grant logic ensures that at any instant only one controller can use the common dataway cycle generator and station decoding circuitry. If the AFC has control then a computer request (PIO or DMA) for the dataway will be delayed by a maximum of 2 $\mu$s until the current dataway cycle is completed. A computer generated "time out" of 5 $\mu$s will automatically complete an unterminated IOB cycle and raise an interrupt at a high priority level (level 14).

The normal grant logic sequence shown below operates on a cyclic and not a priority basis. A maximum of two AFC controllers are permitted in any single crate:

CPU → AFC 1 → CPU → AFC 2 → CPU → AFC 1 .... etc.

(where CPU = PIO or DMA request determined by computer priority).

DMA priority is given to the device closest to the computer. This sequence ensures that the IOB time out is never normally activated. Typical dataway cycle time is set to 1.2 $\mu$s.

In the absence of CPU requests and a permanent request from AFC 1, then these are continuously granted until either CPU or AFC 2 requests appear. AFC operations are not disturbed by LAM demands which are serviced by IOB action because interrupt service does not require use of the CAMAC dataway. Instantaneous requests for PIO, INT or DMA cycles are organized by the computer.

# 4 SUPPLEMENTARY DOCUMENTATION


1) NORD-10 I/O Manual March 1973.

2) ESONE Specification EUR 4100 (1972).

3) ESONE Specification EUR 4600 (1972).

4) Report CERN LAB II/CO/73-1.
(A Multicontroller Approach to CAMAC for the SPS Control System.)

5) CERN LAB II CONTROL GROUP STANDARDS FOR ELECTRONIC EQUIPMENT

6) NORD-10 Reference Manual.

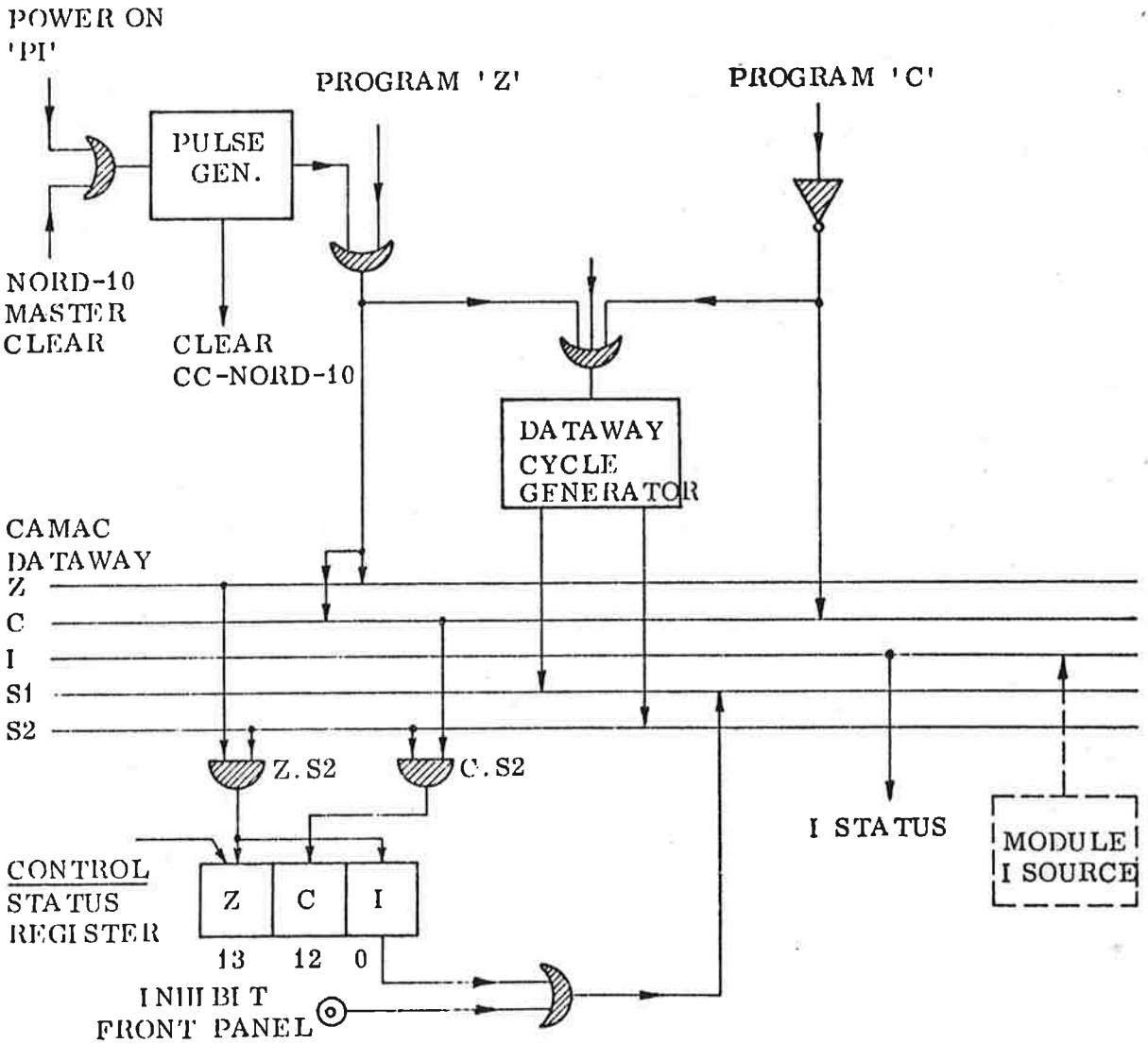
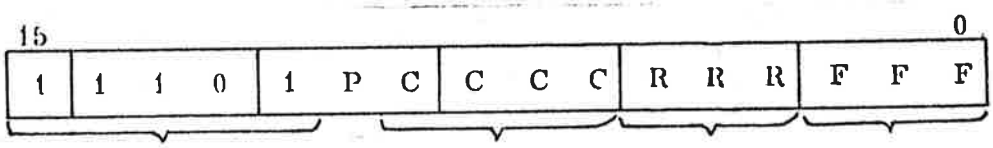




Figure 4.1 - Z, I, C Logic

APPENDIX A

ADDRESSING AND DATA FORMAT

## A.1 IOX Addressing Format for CAMAC




A maximum of 2048 registers may be addressed on the NORD-10 IOB.

P NORD-10 PERIPHERAL TYPE

0 = NORSK DATA PERIPHERALS
1 = CAMAC CRATES

C = CAMAC CRATE ADDRESS 0 - 15

R = CRATE CONTROLLER REGISTER ADDRESS

0 = DATAWAY Z
1 = DATAWAY C
2 = DATA BUFFER
3 = NAF REGISTER
4 = GRADED LAM PATTERN
5 = NOT USED
6 = MASK REGISTER
7 = CONTROL/STATUS (COST)

F REGISTER FUNCTION

0 = ALL REGISTERS - READ
1 = ALL REGISTERS - WRITE
3 = SELECTED BIT CLEAR
5 = SELECTED BIT SET
7 = EXECUTE DATAWAY CYCLE

| REGISTER/FUNCTION | R | F | OCTAL |
|---|---|---|---|
| DATAWAY Z | 0 0 0 | 1 1 1 | 0 7 |
| DATAWAY C | 0 0 1 | 1 1 1 | 1 7 |
| DATA READ | 0 1 0 | 0 0 0 | 2 0 |
| DATA WRITE | 0 1 0 | 0 0 1 | 2 1 |
| DATA EXECUTE | 0 1 0 | 1 1 1 | 2 7 |
| NAF READ | 0 1 1 | 0 0 0 | 3 0 |
| NAF WRITE | 0 1 1 | 0 0 1 | 3 1 |
| NAF EXECUTE | 0 1 1 | 1 1 1 | 3 7 |
| G. LAM READ | 1 0 0 | 0 0 0 | 4 0 |
| MASK READ | 1 1 0 | 0 0 0 | 6 0 |
| MASK WRITE | 1 1 0 | 0 0 1 | 6 1 |
| MASK BIT CLEAR | 1 1 0 | 0 1 1 | 6 3 |
| MASK BIT SET | 1 1 0 | 1 0 1 | 6 5 |
| COST READ | 1 1 1 | 0 0 0 | 7 0 |
| COST WRITE (NOT BIT 9) | 1 1 1 | 0 0 1 | 7 1 |
| COST BIT CLEAR ( - " - ) | 1 1 1 | 0 1 1 | 7 3 |
| COST BIT SET ( - " - ) | 1 1 1 | 1 0 1 | 7 5 |

## A.2 Data Format for CC-NORD-10 Registers

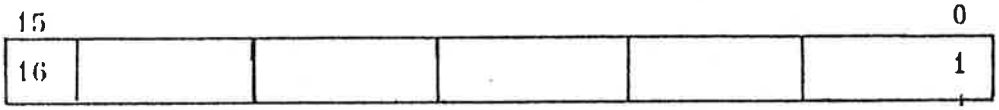
### A.2.1 Dataway Z

NAF and DATA registers are cleared.
COST gets the value 030001.
MASK register remains unchanged.

### A.2.2 Dataway C

NAF and DATA registers are cleared.
Bit 12 in COST is set to 1.

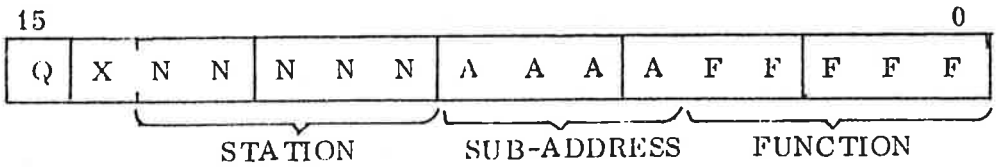
### A.2.3 CAMAC Read/Write Data Register




The data register is used to buffer the CAMAC READ LINES (R1-16) or WRITE LINES (W1-16) during programmed NORD-10 CAMAC READ or WRITE operations. Dataless CAMAC commands do not change the state of the data register, except Z and C cycles. The CC-NORD-10 ignores data on CAMAC READ/WRITE Lines (17-24).

Data may be written into the data register and read back for I/O diagnostics without necessarily executing a CAMAC dataway cycle.

### A.2.4 NAF Register

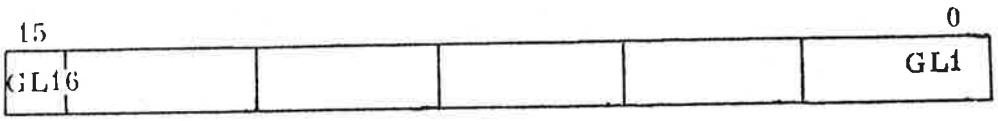



If Q = 1 and/or X = 1 are programmed, then X and Q are automatically checked and can give an error interrupt if this is enabled (see the control register).

For special DATAWAY (clear C) and (Initialize Z) cycles no data is necessary in the NAF register.

## A.2.5 GRADED LAM DATA

GRADED LAM STATUS

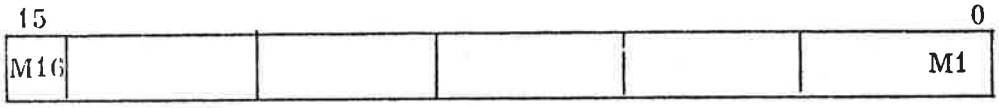



GRADED LAM DATA (GL1-16) is derived directly from the patching of 24 'L' lines in the LAM GRADER. This information is not buffered in the CC-NORD-10.

Enabled LAM sources may become set at any time, but data bits would be reset only under program control.

## A.2.6 LAM Mask Register

MASK DATA



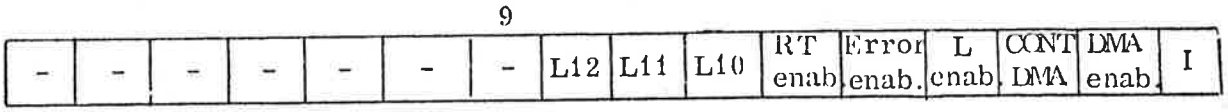

MASK DATA BIT 0 (M1) is used to mask GRADED LAM (GL1).
MASK DATA BIT 15 (M16) is used to mask GRADED LAM (GL16).

MASK BIT SET (M = 1) enables GRADED LAM.
MASK BIT CLEAR (M = 0) disables GRADED LAM.

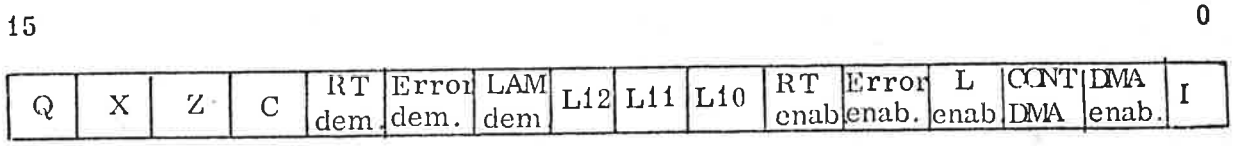
The MASK WRITE operation overwrites all mask data bits.
The MASK READ operation reads all mask data bits.
The MASK BIT SET operation sets selected mask data bits set in the A register.
The MASK BIT CLEAR operation clears selected mask data bits set in the A register.

## A.2.7 CONTROL and STATUS Register (COST)

CONTROL REG.




STATUS REG.




All bits are readable. All bits except bit 9 are writable or may be separately cleared or set.

Bits 12-15 are set at S1 of all programmed dataway cycles. Bit 0 in status is the OR function of all I sources.

CONTROL/STATUS REGISTER - BIT FUNCTIONS - BIT SET/CLEAR CHARACTERISTICS

| BIT | FUNCTION | BIT SET (WCR=WRITE TO CONTROL REG. | BIT TEST READ STAT. REG. | BIT CLEAR (WCR=WRITE TO CONTROL REG.) |
|---|---|---|---|---|
| Q | DATAWAY Q RESPONSE | LAST DATAWAY CYCLE AT S1 OR WCR BIT 15=1 | BIT 15 | NEXT DATAWAY CYCLE OR WCR BIT 15=0 |
| X | DATAWAY X RESPONSE | LAST DATAWAY CYCLE AT S1 OR WCR BIT 14=1 | BIT 14 | NEXT DATAWAY CYCLE OR WCR BIT 14=0 |
| RT DEMAND | REAL TIME INT. STATUS | FRONT PANEL TTL SIGNAL OR WCR BIT 11=1 | BIT 11 | WCR BIT 11=0 |
| RT ENABLE | ENABLE REAL TIME INT. | WCR BIT 5=1 | BIT 5 | WCR BIT 5=0 OR REAL TIME INT. |
| ERROR DEMAND | QX-ERROR INT. STATUS | AT S1 IF ERROR ENABLE =1 AND Q. (NAF 15)+X. (NAF 14)≠1 OR WCR BIT 10=1 | BIT 10 | WCR BIT 10=0 |
| ERROR ENABLE | ENABLE QX-ERROR INT. | WCR BIT 4=1 | BIT 4 | WCR BIT 4=0 OR QX. INT. |
| L DEMAND | CRATE DEMAND STATUS | SET BY UNMASKED LAM IF L ENABLE = 1 | BIT 9 | LAM AUTO-MASK |
| L ENABLE | ENABLE CRATE DEMAND | WCR BIT 3=1 | BIT 3 | WCR BIT 3=0 |
| L12,11,10 | SET CRATE TO INT. LEVEL | WCR BIT 8,7,6=1 | BITS 8,7,6 | WCR BITS 8,7,6=0 |
| CONT DMA | ENABLE DMA BLOCK XFER | WCR BIT 2=1 (BLOCK XFER MODE) | BIT 2 | WCR BIT 2=0 (INTERLEAVED) |
| I | DATAWAY INHIBIT | WCR BIT 0=1, Z OR C CYCLE OR FRONT PANEL SIG. | BIT 0 | WCR BIT 0=0 IF OTHER I≠1 |
| C | DATAWAY CLEAR | SPECIAL IOX (C) OR WCR BIT 12=1 | BIT 12 | NEXT PROGR. DATAWAY CYC. OR WCR BIT 12=0 |
| Z | DATAWAY INITIALIZE | SPECIAL IOX (Z) OR WCR BIT 13=1 | BIT 13 | NEXT PROGR. DATAWAY CYC. OR WCR BIT 13=0 |
| DMA ENABLE | ENABLE DMA XFER | WCR BIT 1=1 | BIT 1 | WCR BIT 1=0 |

APPENDIX B

SUMMARY OF PROGRAMMEABLE OPERATIONS ON CC-NORD-10

1) NORD-10 MASTER CLEAR GENERATES Z ON ALL CRATES AND CLEARS ALL CC-NORD-10 REGISTERS EXCEPT MASK REGISTER.

2) AN IOX EXECUTE INSTRUCTION ALWAYS GENERATES A CAMAC DATAWAY CYCLE.

3) THE LETTER 'C' IN THE IOX ADDRESS INDICATES THE 4-BIT IOX ADDRESS CODE FOR CAMAC CRATE 'C'.

% CAMAC INITIALIZE

```
IOX   2C07    % GENERATE CAMAC 'Z' CYCLE CRATE 'C'
```

% CAMAC CLEAR

```
IOX   2C17    % GENERATE CAMAC CLEAR CYCLE
```

% READ STATUS

```
IOX   2C70    % READ STATUS REGISTER TO CHECK
              % Z, C, I STATUS = 1
```

% CONTROL REGISTER OPERATION

```
SAA   0       % CLEAR A REGISTER
IOX   2C71    % WRITE TO CONTROL REGISTER I = 0
              % TO REMOVE DATAWAY INHIBIT
```

OR BIT CLEAR OPTION MAY BE USED

% CAMAC READ COMMAND

```
LDA   NAFR    % FETCH CAMAC READ COMMAND
IOX   2C37    % WRITE TO NAF REG. EXECUTE
              % CAMAC CYCLE
STA   BUFR    % READ DATA RETURNED TO A REGISTER
```

% CAMAC CONTROL COMMAND + TEST Q

```
LDA   NAFC    % FETCH CAMAC CONTROL COMMAND
IOX   2C37    % WRITE TO NAF. REG. EXECUTE
              % CAMAC CYCLE
IOX   2C70    % READ STATUS REG.
JAP   *-3     % REPEAT CONTROL COMMAND IF Q
              % NOT SET
```

% CAMAC WRITE COMMAND

```
        LDA     DATA    % FETCH CAMAC WRITE DATA
        IOX     2C21    % STORE DATA IN DATA REGISTER
        LDA     NAFW    % FETCH CAMAC WRITE COMMAND
        IOX     2C37    % EXECUTE CAMAC CYCLE
```

OR

```
        LDA     NAFW    % FETCH CAMAC WRITE COMMAND
        IOX     2C31    % STORE IN NAF REGISTER
        LDA     DATA    % FETCH CAMAC WRITE DATA
        IOX     2C27    % EXECUTE CAMAC CYCLE
```

% READ GRADED LAM STATUS

```
        IOX     2C40    % READ GRADED LAM DATA
        JAZ     *-1     % REPEAT UNTIL LAM SET
```

% INTERRUPT HANDLING

% INTERRUPT VECTOR FORMAT = CCCC LLLL
% C = CRATE ADDRESS = 0 - 17 OCTAL
% L = GRADED LAM NO. = 0 - 17 OCTAL

% TYPICAL INTERRUPT HANDLER

```
        IDENT (LEVEL    % SPECIAL IOX GENERATES IDENT
                        % AND RETURNS VECTOR TO A REG.
        COPY  SA DX     % TRANSFER A REG. TO X REG. AS
                        % INDEX
```

% MASK OPERATIONS

```
        IOX     2C60    % READ GL MASK
        IOX     2C61    % WRITE GL MASK
        IOX     2C63    % BIT CLEAR MASK TO DISABLE LAM
        IOX     2C65    % BIT SET MASK TO ENABLE LAM
```