Floppy Disk Controller 3027

ND-11.015.01

NORSK DATA A.S



Floppy Disk Controller 3027

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THE MANUAL

This manual gives a general description of the Floppy Disk Controller -3027. It contains general information on the hardware and the self test feature and explains the read write operations and their associated commands.

THE READER

The manual is written for service personnel and also those who intend to write their own driver routines.

PREREQUISITE KNOWLEDGE

The reader should know the FLOPPY DISK SYSTEM manual (ND.-11.012.01) and the TEST PROGRAM DESCRIPTION (ND-30.005).



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FLOPPY DISK CONTROLLER -3027

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FLOPPY DISK CONTROLLER -3027 GENERAL DESCRIPTION

1.INTRODUCTION

1.1.GENERAL DESCRIPTION

The FLOPPY DISK CONTROLLER -3027 can read/write on single/double density and single/double-sided diskettes. Data transfer and exchanging of commands/status is done with DMA (Direct Memory Access).

The controller is designed and built around the Z80A-microprocessor, the AM9517 DMA controller and the FD1797 floppy disk controller.

The controller is compatible with previous single-sided controllers. For "stand-alone" use, a new version of FLO-MON (FLOPPY-MONITOR-2010F) must be dumped on the diskette.

Possibilities of simulating DMA-loads are implemented, but due to the micro program in the ND-100, this can only be performed from terminal (21560\$) (DMA-load), and not by setting the ALD selector on the CPU module.

When DMA-load is performed, "the first page" on floppy is dumped to "first page" on the ND-100. It is also possible to "load" BPUN-files of maximum 64k words directly from from the floppy by pressing LOAD.

There is a new driver program in the ND-100 which is smaller than those used in previous floppy controllers.



Figure 1. 3027 Floppy Disk Controller.

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FLOPPY DISK CONTROLLER -3027 NORMAL OPERATION

2.NORMAL OPERATION

2.1.READ/WRITE OPERATIONS

When activating for read/write operations follow these steps:

- Enter command block to the ND-100 memory. (Consisting of 6 words - command - diskaddress - DMA address -Word count/number of sectors.) (See also programming example.)
- 2) Load command-block pointers to the controller by means of IOX. (IOX DEVNO+5, IOX DEVNO+7.)
- 3) Activate controller by loading the control word with bit 8 set. (IOX DEVNO+3.)

When the control word is loaded, an interrupt is given to the Z80 processor. A DMA transfer of the command block from the ND-100 to the floppy controllers local memory is initiated. The command is analyzed and executed.

When data transfer has terminated, the status block of 6 words (16 bits) is transferred to ND-100 and placed in memory after the command block.

Finally the "READY-FOR-TRANSFER" signal is set which also gives an interrupt to ND-100 (if interrupt is enabled).

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FLOPPY DISK CONTROLLER -3027 HARDWARE

3.HARDWARE

3.1.STANDARD HARDWARE

The controller is equipped with standard IOX and DMA logic. IOX numbers can be found in the programming examples.

It is possible to choose between the device numbers 1560 and 1570. They are represented by 0 and 1 respectively on the thumb wheel.

Converting 16-bit words to bytes is done during the DMA transfer of a sequence made up of a PAL10L8 (which is of PROM-type) and two flipflops. Internaly this module has an eight bit bus. Normally, there will be 6 kbyte PROMs and 4 kbyte RAMs, both of which can be extended easily to 8 kbytes by adding more circuits.

A CMOS counter controls the time-out function. It is set when loading the control word and reset each time data is transmitted between the floppy drive and the controller. Time-out after approximately 10 seconds.

A new feature added on this controller is a hardware compare circuit which verifies data read from or written to the diskette.

The control part of the floppy is taken care of mainly by FD1797 circuits delivered by Western Digital. This circuit does most of the control functions. The synchronizing and separating of data and clock, however, must be done outside this circuitry in a data separator.

The data separator consists of an analog phase locked loop, and some circuitry to compensate for loss of time margin in the floppy control circuit.

Precompensation is done outside FD1797 and may be turned ON/OFF from the processor.

Error codes are shown on a display at the edge of this module. The codes shown are the same as the codes returned in statusword 1 (bit 9-15).

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FLOPPY DISK CONTROLLER -3027 TESTING

4.TESTING

4.1.SELF-TESTING

When an MC (MASTER CLEAR) pulse is given to the floppy controller the processor will perform a self-test. This can be observed on the error display which is first "turned OFF", then set to 000 upon successful completion of the test. During selftest, drive 0 is selected and restored.

Upon detection of errors the codes E70-E75 are displayed. If the display is not lit or shows codes other than the ones specified, the processor will not be able to perform a selftest.

The phases of the selftest are as follows:

- 1. The proms are read and a checksum is calculated. This checksum should be equal to 55H (H = hexadecimal).
- 2. A RAM test is performed.
- 3. The Z80A-CTC (timer/interrupt controller) is tested.
- 4. The DMA-controller AM9517-4 is run in testmode.
- 5. The VCO SN74LS629 is measured and adjusted to be within the limits of the phaselocked loop.
- 6. A test of the floppy controller chip FD1797.

4.2.RAMTEST

The part of the RAM being used for buffering of data from/to the floppy disk will be tested continuously. The test starts when the controller has been idle for approximately 3 minutes.

This is a comprehensive test that uses approximately 30 minutes to test 1Kbyte.

A new access from the ND-100 will stop the test.

<u>NOTE:</u>If errors are discovered during selftest or RAM test the controller will not carry out commands. This to prevent destruction of data on the diskettes.

Bit 4 and 7 in the status word (hardware) will be set. The status field will not be written to the ND-100 memory. The status word 1, however, will be written to the controller data register and may be read from this (IOX DEVN0.+0).

4.3.TEST OPTIONS

A total of 24 different tests are supported by the microprocessor program (see specification).

This should make it easy to write test and maintenance programs.

As an example, the T13 makes it possible to write a Z80 program, load it from ND-100 to the local RAM and start program execution by T15. T7 -T8 -T24 makes it possible to read and write to all registers in the controller.

5.COMMANDS

5.1.READ DATA

Data is read from the floppy disk to the ND-100 memory. The start address is given as the logical sector address, and a choice can be made between the wordcount and the number of sectors to indicate the length of the transfer.

NOTE: The transfer will always start at the beginning of a sector, but the number of words to be read may be preset to any number of words.

5.2.WRITE DATA

Same procedure as READ DATA, except that transfer is now from ND-100 to the diskette.

5.3.FIND EOF

Same procedure as READ DATA, except that data is only read to the local buffer. There is no transfer to ND-100, except for the status. Bit 5 in status word 1 indicates if it is an EOF (deleted record).

5.4.WRITE EOF

The sector given in the command block is read to the local memory and written back as a deleted record.

FLOPPY DISK CONTROLLER -3027 COMMANDS

5.5.FORMAT FLOPPY

The floppy disk placed in the specified drive is formatted to the format given in the command word.

5.6.READ FORMAT

The format is read from the floppy disk and returned to status word two. The disk address and the format of the command field indicates where the format should be read.

5.7.READ DELETED RECORD

Reads data from a record marked as a deleted record, and transfers them to ND-100.

5.8.WRITE DELETED RECORD

Writes a record from ND-100 and marks it as a deleted record.

5.9.COPY FLOPPY

Copies from one drive to another. The entire floppy is copied.

FLOPPY DISK CONTROLLER -3027 COMMANDS

5.10.FORMAT TRACK

One track on one side is formatted. This command can be used to make IBM compatible diskettes.

NOTE: The track address must be given as logical address to the first sector of the track.

5.11.CHECK FLOPPY

Data is read to the controllers local memory to test for CRC-errors. The test halts with the first discovered error. The address of the erroneous sector is held in LAST MEMADR. in the status field.

STATUS FIELD:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Side	Track number						Sec	eto	or	nι	ımt	ber	1			

6.PROGRAMMING SPECIFICATIONS

6.1.IOX-NUMBERS

DEVNO +	0	- READ DATA
DEVNO +	1	- NOT USED
DEVNO +	2	- READ STATUS
DEVNO +	3	- LOAD CONTROL WORD
DEVNO +	4	- READ STATUS
DEVNO +	5	- LOAD POINTER HIGH (BIT 16-23)
DEVNO +	6	- NOT USED
DEVNO +	7	- LOAD POINTER LOW/LOAD DATA

6.2.THUMBWHEEL SETTINGS

2-1	5	-	NOT	USE	D
1	-		DEVI	10	1570
0	-		DEVI	10	1560

6.3.COMMAND ADDRESS BLOCK & STATUS BLOCK



POINTS TO NOTE:

IF WC/SC - 1. - WORDCOUNT IF " 0. - SECTORCOUNT

DISK ADDRESS: INDICATES THE START ADDRESS ON THE FLOPPY DISK. THIS IS GIVEN AS A LOGICAL SECTOR ADDRESS, STARTING WITH TRACK 00, SIDE 0, SECTOR 1 WHICH IS ADDRESS 0 AND INCREASING TO THE MAXIMUM NUMBER OF SECTORS.

MEM. ADDRESS: INDICATES WHERE TO START IN THE ND-100 MEMORY.

WORD/SECT COUNT: WC/SC = 1 INDICATING WORD COUNT (=24 BIT) WC/SC = 0 INDICATING SECTOR COUNT (NUMBER OF SECTORS TO BE TRANSFERRED). IF THE WORD COUNT IS LESS THAN THE NUMBER OF WORDS IN A SECTOR, THE TRANSFER WILL START AT THE BEGINNING OF THE SECTOR.

ND-DUAL-DENSITY-FORMAT = 8 (SECT) X 77 (TRACKS) X 2 (SIDES)

6.4.STATUS WORD 1 - 3027B



6.5.STATUS WORD 2 - 3027B

BIT			
0 1 2 3 4 5 6	BYTES SECTOR DOUBLE SIDED DOUBLE DENSITY NOT USED NOT USED NOT USED	FORMAT READ FROM DISKETTE VALID FOR READ FORMAT COMMAND OR WHEN ERROR 12	2
7 8 9 10 11 12 13 14 15	NOT USED SELECTED UNIT SELECTED UNIT NOT USED NOT USED NOT USED NOT USED NOT USED		

6.6.HARDWARE - CONTROL WORD

IOX (DEVNO. + 3) BIT 0 NOT USED 1 ENABLE INTERRUPT ON RFT 2 ACTIVATE AUTOLOAD 3 TEST MODE 4 DEVICE CLEAR 5 6 NOT USED NOT USED 7 NOT USED 8 EXECUTE COMMAND 9 IF BIT 8=1 : STEP RATE IF BIT 3=1 10 AND BIT 3=0: IN USE THEN BIT 11 : DISABLE PRECOMP BIT 9-13 ARE 12 : 96 TPI (144 TRACK) TESTSPECS 13 : COMPARE 14 NOT USED 15 NOT · USED

6.7.HARDWARE - STATUS WORD

IOX (DEVNO + 2)

BIT	
0	NOT USED
1	RFT - INTERRUPT ENABLED
2	DEVICE ACTIVE
3	DEVICE READY FOR TRANSFER
4	OR OF ERRORS
5	NOT USED
6	NOT USED
7	HARDERROR - DMA TRANSFER
0	
10	
11	NOT USED
12	CNOT USED
13	
14	
15	1- HIGH=DUAL DENSITY CONTROLLER

6.8.COMMAND WORD

15 14	13 12	11	10 9 1	8	7 6	5 4 3 2	1 0
COPY DEST.	N.U.	F	ORMAT		UNIT	FUNCTION	
		D E N S T	S I D E				
		T Y	2				

BIT 0-5:	OCTAL	HEXA	FUNCTION
	0	0	READ DATA
	1	1	WRITE DATA
	2	2	FIND EOF (READ WITHOUT DATATRANSFER)
	5	5	WRITE EOF (WRITE DELETED RECORD)
	41	21	FORMAT FLOPPY
	42	22	READ FORMAT
	43	23	READ DELETED RECORD
	44	24	WRITE DELETED RECORD
	54 55 56	- 2C 2D 2E	COPY FLOPPY Format track Check floppy
BIT 6-7:	0	0	SELECT UNIT 0
	1	1	SELECT UNIT 1
	2	2	SELECT UNIT 2
	3	3	SELECT UNIT 3
BIT 8-11:			FORMAT

BIT:	9	8	3
1	0	0	512 BYTES/SECTOR
	0	1	256 BYTES/SECTOR
	1	0	123 BYTES/SECTOR
	1	1	1024 BYTES/SECTOR

Sec.

BIT:	11	
	0	SINGLE DENSITY
	1	DOUBLE DENSITY

BIT: 12-13 N	IOT 1	USED
--------------	-------	------

BIT: 14-15 COPY DESTINATION

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6.9.ERRORCODES

OCTAL	
00 05	OK CRC ERROR
06	SECTOR NOT FOUND
07	TRACK NOT FOUND
10	FORMAT NOT FOUND
11	DISKETTE DEFECT (IMPOSSIBLE TO FORMAT)
12	FORMAT MISMATCH
13	ILLEGAL FORMAT SPECIFIED
14	SINGLE SIDED DISKETTE INSERTED
15	DOUBLE SIDED DISKETTE INSERTED
. 16	WRITE PROTECTED DISKETTE
17	DELETED RECORD
20	DRIVE NOT READY
21	CONTROLLER BUSY ON START
22	LOST DATA (OVER OR UNDERRUN)
23	TRACK ZERO NOT DETECTED
24	VCO FREQUENCY OUT OF RANGE
25	MICROPROGRAM OUT OF RANGE
26	TIMEOUT
27	UNDEFINED ERROR
30	TRACK OUT OF RANGE
31	
32	COMPARE ERROR (DURING COMPARE OF DATA)
33	INTERNAL DMA ERRORS
34	
35	
36	
37	

40 41 42 43 44 45 46 47	ND-100 BUS ERROR COMMAND FETCH ND-100 BUS ERROR STATUS TRANSFER ND-100 BUS ERROR DATA TRANSFER ILLEGAL COMMAND WORDCOUNT NOT ZERO
50 51 52 53 55 55 56 61 62 63 64 56 66	NO BOOTSTRAP FOUND ON DISKETTE WRONG BOOTSTRAP (TOO OLD FLO-MON VERSION)
67 70 71 72 73 74 75 76 77	PROM CHECKSUM ERROR RAM ERROR CTC ERROR DMACTRL ERROR VCO ERROR FLOPPY CONTROLLER ERROR

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FLOPPY DISK CONTROLLER -3027 TEST MACROS

7.TEST MACROS

7.1.HARDWARE CONTROLWORD IN TESTMODE

The floppy controller has a program containing various test routines. These routines can be activated from the ND-100. It is done by setting bit 3 in the control word. This indicates that bits 9-15 have a special meaning. They will contain the number of the test to be activated.

The significance of the contents of registers POH, POM and POL will vary with the different tests. However, it will normally be these registers that are used to transfer parameters used in the testing. This avoids using the COMMAND FIELD in memory.

The tests T13 and T14 are exceptions. They use a field in the ND-100 memory to specify addresses and bytecount when loading program/data to/from the ND-100.

The tests T13, T14, T16, T17 and T18 will write the status word 1 to the data out register. This register can be read with the IOX READ-DATA.

7.2.TEST ROUTINES IN THE FLOPPY CONTROLLER

BITS 0 - 8 STANDARD (WHEN TEST BIT 3 IS SET) BITS 9 - 15 SPECIFY TEST

The tests and the control words are given on the following page.

TEST	CONTROLWORD	ACTION
то	00041X`	DO NOTHING (SET RFT)
T1	00141X	STOP CONTROLLER (TEST TIMEOUT)
Т2	00241X	DATA INPUT REGS. (POL & POM) ARE COPIED TO DATAOUT
m -2	00011477	REGISTERS (DLO & DHI).
13	00341X	DOH IS COPIED TO DLO (BITS 0-7)
14	00441X	POH IS COPIED TO ADDRESS GIVEN BY POL & POM
15 T6	00541X	MEM SIZE (UDDED ADDRESS IN DAM) LOADED TO DOL & POM
10 T7	00741	MEM. SIZE (UPPER ADDRESS IN RAM) LUADED TO POL & POM
т8 Т	01041x	DIO LOADED WITH CONTENTS OF PEC ADDRESSED BY DOL
T 9	01141X	DMA INPUT TEST (Z80 ND 100)
-,		POH = BLOCK NUMBER IN Z80 MEMORY
1		BLOCK 1 STARTS AT 2000H IN CONTROLLER
li li	÷	POL & POM = ND-100 ADDRESS (ONLY FIRST 64K WORDS
		ARE USED)
		Z80 ADDR.= 2000H+[128.(POHI-1)]
T10	01241X	DMA OUTPUT TEST (ND-100-Z80)
		PARAMETER SAME AS T9
T11	01341X	COMPARE TEST POL & POM = START ADDRESS
		COMPARE IN THE Z80 MEMORY THE TWO FOLLOWING BLOCKS
		OF 128 BYTES.
1		DLO & DHI = REMAINING BYTES AFTER COMPARE ERROR
TT 12	01/01/17	IF DLO & DHI = U THEN OK
T12	015/117	DISPLAT TEST. DISPLAY COUNT FROM 0 TO 9
212	015412	ADDRESS IN ND 100 AND 790 HORDONNE TO DEFENSE
		FROM ND_100 MEMORY
		POH. POM & POL ARE POINTERS TO PARAMETER ETELD
		(SEE ALSO NEXT PAGE FOR THIS TEST)
T14	01641X	LOAD TO ND-100 FROM Z80 (PARAMETER SAME AS T13)
T15	01741X	START PROGRAM IN ADDRESS GIVEN BY POL & POM
T16	02041X`	GENERATE CRC ERROR ON; POL = SECTOR NUMBER,
		POL = TRACK, POH = DEVICE-SEL-REG. (FDVSEL)
T17	02141X	DESTROY TRACK; POM = TRACK, POH = DEV-SEL-REG.
T18	02241X	DESTROY 1 SECTOR
T 10	00011477	POM = TRACK, POH = DEV-SEL-REG.
T19 T20	02341X	TAP-TAP TEST. POH = NUMBER OF TAPS.
T21	02441	SIOP DISPLAY
T22	02541	CHANGE TO INTERRUPT ADDRESS IN PROM (FOR RAM TEST).
T23	027418	READ STACKPOINTER (FUL & FUM = VALUE)
T24	03041x	EXECUTE ED 1797 COMMAND
		POH = FD1797 TRACK REGISTER
		POL = FD1797 COMMAND REGISTER
		WHEN FINISHED: POM = FD1797 TRACK-REG
		POL = FD1797 - STATUS
	9	

<u>NOTE:</u> IF X = 0, NO INTERRUPT - IF X = 1 INTERRUPT WHEN FINISHED

FLOPPY DISK CONTROLLER -3027 TEST MACROS

7.3.ADDRESS FIELD FOR UP DOWN LOAD

(USED FOR T13 AND T14)

IN Z80 RAM:

20 F2H	ND-100 LOAD ADDR
20F1H	ND-100 LOAD ADDR
20F2H	Z80 ADDR
20F3H	Z80 ADDR
20F4H	BYTECOUNT
20F5H	BYTECOUNT
	8 BITS

IN ND-100:

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POL, POM AND POH POINTS TO ADDRESS-FIELD
7.4. READING THE MICRO-PROGRAM VERSION NUMBER

When the microprogram is changed it will be given a new version number. This is done by adding a letter (A-Z) after the PROM number.

The PROM will also contain a counter that will keep track of the version and this counter can be read by running test 5 (T5).

The PROM number, contained in address 60H, is given as 0, 1, 2....,where A=0, B=1, C=2 and so on. The version may be read as follows (ND-100 program):

SAA	140 % Address 60H in
IOX	DEVNO+7 % Z80 Memory
LDA	(5410 % Test number 5
IOX	DEVNO+3
IOX	DEVNO+2 🖇 Wait until
BSKP	ZRO 20 DA 🖇 ready
JMP	*_2
IOX	DEVNO+0
WAIT	% A-register contains
)FILL	% when micro program
	% version number

8.REGISTERS IN THE FLOPPY CONTROLLER

Description of the various registers in the DMA controller AM9517, the floppy controller FD1797, the counter-timer Z80-CTC and the digital/analoge converter AD558 can be found in the respective databooks.

NAME	REGISTER	FUI	NCTIO	N		VALUE	(HEX)	VALUE	(OCT)
CNB	CTC-CHNL	0:	INT:	FROM	ND-100		10		20
CCP	CTC-CHNL	1:	INT:	FROM	HARD-COMPARE		11		21
CFC	CTC-CHNL	2:	INT:	FROM	FLOPPY-CONTR		12		22
CDMA	CTC-CHNL	3:	INT:	FROM	DMA-CONTR		13		23

DMA CONTROLLER

DCOM	COMMAND REGISTER	28	50
DMOD	MODE REGISTER	2B	53
DRQ	REQUEST REGISTER	29	51
DMSK	MASK REGISTER (WRITE BIT)	2A	52
DMSKW	MASK REGISTER (WRITE ALL BITS)	2F	57
DTEMP	TEMPORARY REGISTER	2D	55
DST	STATUS REGISTER	28	50
DMC	MASTER CLEAR (PROGRAMMED)	2D	55
DCFF	CLEAR INTERNAL FLIP-FLOP	2C	54
DADR	ADDRESS REGISTER CHANNEL O	20	40
DWC	WORD COUNT CHANNEL O	21	41

ND-100 BUSCONTROL

4.5.7		-	
ADL	DMA ADDRESS BITS 0-7	50	120
ADM	DMA ADDRESS BITS 8-15	51	121
ADH	DMA ADDRESS BITS 16-23	52	122
RWFF	READ OR WRITE DMA	53	123
DLO	DATA OUT BITS 0-7	54	124
DHI	DATA OUT BITS 8-15	55	125
SDISP	DATA TO DISPLAY (7 SEG)	56	126
FINI	SET RFT AND STATUS (FINISH)	57	127
TRST	TRANSFER STATUS REGISTER (DMA)	50	·
120			
POL	POINTER OR DATA-IN BIT 0-7	51	121
POM	POINTER OR DATA-IN BIT 8-15	52	122
POH	POINTER ADDRESS BITS 16-23	53	123
CW	CONTROLWORD	54	124

FLOPPY CONTROLLER

	FCCOM	COMMAND REGISTER	70		160
	FCST	STATUS	70	62	160
	FCTRK	TRACK	71		161
Ì	FCSEC	SECTOR	72		162
i	FCDAT	DATA	73		163
	FDVSEL	DEVICE SELECT AND MODE	74		164
-	FCCLR	FLOPPY CONTROLLER CLEAR	75		165
]	FADC	DIGITAL/ANALOG CONVERTER	76		166
1	FDST	FLOPPY DRIVE STATUS	77		167
]	DMREG	DISPLAY AND MODE REGISTER	40		100

8.1.RWFF - REGISTER

DMA DIRECTION

BIT O	:	0	DMA	TO NI	0–100
11	:	1	DMA	FROM	ND-100
BIT 1-7	:	N	OT US	SED	

8.2.FINI - SET RFT AND STATUS

BIT 0 : OR OF ERRORS (BIT 4 IN HARDWARE STATUS WORD) " 1 : HARDERROR (BIT 7 IN HARDWARE STATUS WORD) BIT 2-7 : NOT USED

NOTE: RFT IS ALWAYS SET WHEN WRITING TO THIS REGISTER.

8.3.TRST - TRANSFER STATUS REGISTER

" 1 - ERROR ON LAST TRANSFER IF SET TO C	BIT	0	-	DMA TRANSFER FINISHED WHEN ZERO (ONE WORD FINISHED)
2-7 - TIED LOW	11	1 2_7	-	ERROR ON LAST TRANSFER IF SET TO ON

NOTE: THIS REGISTER SHOULD BE ZERO AFTER A SUCCESSFUL DMA TRANSFER.

8.4.SDISP - SET DATA TO DISPLAY



THE DISPLAY CONTAINS 3 NUMBERS. THE NUMBER TO BE LIT IS . SELECTED BY LOADING DMREG.

8.5.DMREG - DISPLAY AND MODE REGISTER

BIT	0-2	NOT USED
17	3	PRECOMPENSATION (0=OFF, 1=ON)
11	4	NOT USED
11	5	SELECT FIRST NUMBER IN DISPLAY
11	6	" SECOND NUMBER IN DISPLAY
17	7	" THIRD NUMBER IN DISPLAY

8.6.FDVSEL - DEVICE SELECT AND MODE REGISTER

BIT	0		SELECT DRIVE O
11	1	-	" 1
	2	-	" 2
	3	-	" 3
17	4	-	SELECT DENSITY (DUAL=0, SINGLE=1)
17	5	-	ENABLE COMPARE CIRCUIT
11	6	-	ENABLE VCO ADJUSTMENT
11	7	-	SET IN-USE-LINE

8.7.FCCLR - REGISTER

USED TO PRODUCE A CLEAR PULSE FOR THE FD1797, NO DATA REQUIRED.

8.8.FDST - FLOPPY DRIVE STATUS

READ THE STATUSLINES FROM THE SELECTED DRIVE;

BIT	0	-	READY
11	1	- 1	DOUBLESIDED DISKETTE
11	2	-	DISK CHANGED WHILE SELECTED
19	3	-	ON TRACK OO
11	4-7	-	NOT USED
1.5			

ALL BITS ARE TRUE WHEN ZERO

8.9.CW - REGISTER

HARDWARE CONTROL WORD TRANSFORMED AND READ INTO 280.

BIT	0	-	LOAD FLOMON TO ND-100
**	1	-	GET COMMAND FROM ND-100
п	2	-	TEST MODE
	3	-	STEP RATE
=	4	-	IN USE
**	5		DISABLE PRECOMPENSATION
17	6	-	96 TPI (144 TRACK)
17	7	-	COMPARE

BIT	3		
H	4		
17	5	-	TEST SPECIFICATIONS IF BIT 2=1
11	6	-	NOT USED IF BIT 0=1

8.10.FLAGREGISTERS IN FDTFI

FLOFLG: (IX+OEH)



LFLAG: (IX+ODH)



ERRFLG: (IX+IDH)



8.11.FLOPPY - DATAFIELD

FDTFI:

BYTSEC:

125	-2	NOROT	NUMBER OF ROTATIONS BEFORE LAST DESELECT								
	-1	LSEL	LAST DEVICE SELECT								
	0	TRRG O	TRACK REGISTER DRIVE O								
	1	TRRG 1	1								
	2	TRRG 2	2								
	3	TRRG 3	3								
	4	SDEV	SOURCE DEVICE								
150	5	SDVSEL	SOURCE DEVICE SELECT REGISTER								
	6	DEV	CURRENT DEVICE (CODED)								
	7	DVSEL	CURRENT DEVICE SELECT REGISTER								
	8	LTRACK	LAST TRACK								
	9	LSIDE	LAST SIDE								
	A	LSECT	LAST SECTOR								
	В	LCOM	LAST COMMAND ISSUED								
	С	LSTAT	LAST STATUS READ								
	D	LFLAG	LOCAL-FLAGS USED BY FLODR								
	Ē	FLOFLG	FLOPPY FLAG REGISTER								
	F	GRETR	GENERAL RETRY COUNTER								
	10	FORMCO	FORMAT FROM COMMAND								
	11	FORMRD	FORMAT READ FROM FLOPPY								
	12	SELLEN	SECTOR LENGTH CODE								
	13	SECTR NUMBER OF SECTORS/TRACK									
	14	LOBYTSEC NUMBER OF BYTES/SECTOR									
	15	HIBYTSEC	NUMBER OF BYTES/SECTOR								
	16										
	17										
	18	NFORRD	READ FORMAT IN								
	19	3	ND-100 CODE								

	1A 1B 1C	FSTEP	STEPPING RATE	
	1D 1E 1F 20 21 22	ERRFLG RRETRY STPCT NXRD NXWR BUFFUL DFLAG	FLAGGING VARIOUS ERRORS RESTORE RETRY STEP-IN COUNTER NEXT BUFFER TO BE READ NEXT BUFFER TO BE WRITTEN NUMBER OF BUFFERS FULL	
NOSEC	24 25 26	DRETRY BUFNO LNOSECT	RETRYCOUNTER DMA NUMBER OF BUFFERS (RAM) NUMBER OF SECTORS TO	
REMSEC	27 28 29	HNOSECT REMSEC	BE TRANSFERRED REMAINING SECTORS	
	2A 2B 2C 2D 2E 2F			
	2130 2131 2132 2133 2133 2134	DDEV DDVSEL DTRACK DSIDE DSECT	DESTINATION DEVICE (COPY) DEVICE SELECT REGISTER DESTINATION TRACK DESTINATION SIDE DESTINATION SECTOR	COPY

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8.12.MEMORY ORGANISATION -3027

(H = HEXADECIMAL)





RAM 1 LAYOUT (2000H TO 27FFH)

8.13.ND-100 DOUBLE DENSITY FLOPPY FORMAT



GAP 4A	SYNC	PRE I.AM	I. AM	GAP 1	ID SYNC	PRE ID.AM	AM	ID	CRC	GAP 2	DATA SYNC	PRE D.AM	AM	DATA	CRC	GAP 3	GAP 4B
4E	00	C2*	FC	4E	00	A1#	FE			4E	00	A1#	FB	40		4E	4E
80	12	3	1	50	12	3	1	4	2	22	12	3	1	1024	2	116	654

REPEATED 8 TIMES/TRACK

* - C2 WITH MISSING CLOCK BETWEEN BIT 3 & 4. (DATA=C2, CLOCK=14)
- A1 ______ BIT 4 & 5. (DATA=A1, CLOCK=OA)

TRACKS ARE NUMBERED FROM 0 TO 76 (TOTAL OF 77 TRACKS). SECTORS ----- 1 TO 8 (TOTAL OF 8 SECTORS/TRACK). SIDES ----- " ----- 00H AND 01H.

NOTE: ALL TRACKS ON BOTH SIDES HAVE THE SAME FORMAT, THAT IS -TRACK OOH SIDE OOH AND TRACK OOH SIDE O1H BOTH HAVE 8 SECTORS OF 1024 BYTES.

PAGE	POSITION	TIME	COMPONENT & VALUE	COMMENTS			
1	20	1us	R27=10K, C16=220pF	MASTER CLEAR PULSE			
5	25D	35-50ms	R41=27K, C19=2,2uF	TO CONTROLLER HEAD LOAD DELAY (SETTLETIME ON DRIVE)			
5	25D	50-80us	R42=82K, C20=10nF	RESET PULSE TO FLOPPY CHIP (FD 1797)			
5	4E	0,5us	R39=3,3K, C22=220pF	READ PULSE DUAL DENSITY			
5	4E	1,0us	R40=6,8K, C23=220pF	READ PULSE SINGLE DENSITY			
5	15D	150 - 200ns	R45=220 , C25=470pF	READ DATA TO FLOPPY CHIP			
5		40ns	C26 AND C27	DELAY TO COMPENSATE FOR LOST MARGIN IN FD1797			
5	26E	200- 300ns	R44=680 , C24=680pF	WRITE DATA PULSE			
5	27F	120- 180ns	R43=390 , C21=330pF	PRECOMP TIME			

8.14.ONE-SHOTS AND RC-DELAYS ON THE FLOPPY DISK CONTROLLER

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Figure 2. Registers and Buses in the ND-100 Interface.

APPENDIX A

MICROPROGRAM (FLOW) FOR FLOPPY-DISK-CONTROLLER

(Second Second



FLMIC: MICROPROGRAM FOR FLOPPY-DISK-CONTROLLER

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1









ND-11.015.01

ZECONTRA







ND-11.015.01



IF BIT 2 IN THE CONTROLLWORD IS SET THEN LOAD IS EXECUTED





ND-11.015.01





ND-11.015.01



> <u>DMA-LOAD</u>: 1024 WORDS IS LOADED FROM START OF THE DISKETTE TO ADR 00000g IN ND100 BY WRITING 21560 \$, ON THE CONSOLETERMINAL.

DML PREPEAR LOAD INIT 64K MEMORY READ ONE K. WORDS FROM FLOPPY ADRO TO NOTOO ADRO SRFT [GO TO SET RET ROUTINE]

Appendix A MICROPROGRAM (FLOW) FOR FLOPPY-DISK-CONTROLLER



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ND-11.015.01



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